Analysis of Jitter due to Power-Supply Noise in Phase-Locked Loops

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Abstract- Phase-locked loops (PLL) in RF and mixed signal VLSI circuits experience supply noise which translates to a timing jitter. In this paper an analysis of the timing jitter due to the noise on the power supply rails is presented. Stochastic models of the power supply noise in VLSI circuits for different values of on-chip decoupling capacitances are presented first. This is followed by calculation of the phase noise of the voltage-controlled oscillator (VCO) in terms of the statistical properties of supply noise. Finally the timing jitter of PLL is predicted in response to the VCO phase noise. A PLL circuit has been designed in 0.35μ CMOS process, and our mathematical model was applied to determine the timing jitter. Experimental results prove the accuracy of the predicted model.

I. INTRODUCTION

PLLs are ubiquitous in RF and mixed signal circuits. They are utilized as on-chip clock frequency generators to synthesize the higher internal frequency from the external lower frequency. In data communications and disk drive read channels PLL, systems are also used as clock recovery systems. In all of the above applications, the random temporal variation of the phase, or jitter, is a critical performance parameter. Excessively large jitter consumes some of the clock budget and it can cause error propagation as well as intercommunication errors between chips. The PLL circuit operates from the same supply busses that provide the required voltage to other building blocks of the chip, thus it is subject to supply noise.

The power supply noise is the switching noise on the power supply line which consists of the resistive *IR* drop due to wire resistances and inductive ΔI-noise due to the chip-package wire inductance. In today's deep submicron design with smaller feature size, faster switching speeds, the on-chip inductance is also becoming significant inductive component. There have been several works on power-supply noise analysis[1],[2],[3],[4]. The power supply noise may drive the VCO of the PLL away from its correct frequency, causing the unwanted random uncertainty in frequency. In the meantime, the supply noise affects the performance of the phase detector and the loop filter (*cf.* Fig. 1.). In most clock synthesis applications, a VCO is locked to a very low jitter reference input signal generated by a crystal. With a careful design of PLL building blocks, the noise contribution of phase detector, the frequency divider, and the loop filter can be reduced to a tolerable level. The dominant noise is thus the phase noise of the VCO. Recently there have been some works on characterizing the phase noise in electrical oscillators [5], [6]. Paper [7] attempts to analyze the timing jitter of oscillators due to the power supply and substrate noise. The oscillator subject to supply noise is considered as a VCO with different control voltages and therefore the jitter effect is viewed as frequency-modulated sinusoidal waveform. This paper, however, suffers from one drawback. The VCO system is treated as a deterministic system in the presence of noise.

The goal of the present paper is to predict the timing jitter of a PLL using a more accurate model for the phase-lock loop in terms of the jitter in the VCO resulting from the power supply noise. We focus on the charge-pump PLL due to its widespread application in today's frequency synthesizers and clock generators for microprocessors. Section II briefly explains the block diagram of the PLL system in the presence of all the relevant noise sources. Section III gives a statistical modeling of the power supply noise. Section IV relates the VCO noise to the power supply statistical properties. Then section V formulates the effect VCO noise source on the output phase of the PLL. In section VI the PLL jitter analysis applies on a PLL circuit. Finally section VII concludes our analysis.

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II. SYSTEM MODELING FOR PLL NOISE ANALYSIS

The functional block for a phase-lock loop along with various random noise sources is shown in Fig. 1. In general all the loop components may contribute to the output noise and accumulated jitter.

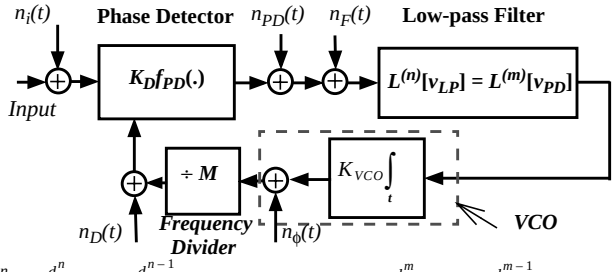

Fig. 1. The functional block diagram of PLL in the presence of all the relevant sources.

The effect of noise on the phase detector performance has been studied in [8] and in any case phase detectors are not a major source of noise in a PLL. The passive low pass filter introduces thermal and shot noise. The timing jitter due to these device noise sources turns out to be significantly less than that due to substrate and supply noises [7]. As a result, timing jitter is mainly associated with two important noise sources:

- noise at the input,
- phase noise of the VCO.

The loop frequency bandwidth of the system determines which noise source has more impact on the timing jitter of the output. A narrow loop-bandwidth reduces the impact of the phase noise at the input on the jitter. Previously more attention has been paid to understanding the effect of the input noise source compared to the VCO phase noise. Furthermore for both clock synthesizers and high performance clock recovery systems an accurate analysis of the output jitter due to the internal VCO phase noise is important. In this paper, we focus on the VCO phase noise injection into the PLL closed loop system.

Let's consider the general case of a PLL shown in Fig. 1. with the nth-order low-pass filter (*LPF*) in place, the differential equation relating the synthesized excess phase and the input phase is as follows:

$$L^{(n)}\left[\frac{d\Phi}{dt}\right] = L^{(n)}\left[\frac{d\theta_{in}}{dt}\right] - L^{(n)}\left[\frac{dn_\phi}{dt}\right] - GL^{(m)}[f_{PD}(\Phi)] \qquad (1)$$

where Φ is the closed-loop phase error, θ_{in} is the input reference phase, G is the closed loop gain constant, $f_{PD}(\Phi)$ represents the phase detector function, $n_\phi(t)$ is the phase noise source of the VCO.

III. POWER SUPPLY NOISE ANALYSIS

A power supply distribution model must include the chip-package-interface power distribution model, the on-chip power bus model,

and an equivalent circuit to represent the switching activities in various functional blocks. The package-level model is mainly dominated by the large chip-package interface inductance, the on-chip power bus model is dominated by the wire resistance. The noise introduced by simultaneous switching of the output drivers can be very large since driving large external capacitances generates large current surges. Fig. 2.a. depicts the HSPICE simulation of the *P/G* bounce due to simultaneous switching of five off-chip drivers without using the decoupling capacitor. Fig. 2.b shows the supply noise in the presence of an on-chip decoupling capacitor of 10pF across each output buffer. The device model parameter is taken from *TSMC 0.25*µ single-poly, five-metal process technology provided by MOSIS which uses **BSIM3v3** MOS model. The main effect of the on-chip decoupling capacitor is that it forces the same fluctuations to appear on both the on-chip power and ground wires. If the decoupling capacitor is made much larger than the switched capacitances, then the on-chip switching noise can be effectively eliminated. Adding the decoupling capacitor, however, is less efficient for most off-chip drivers [3]. Therefore the circuit will always experience the bounce effect on the power and ground busses.

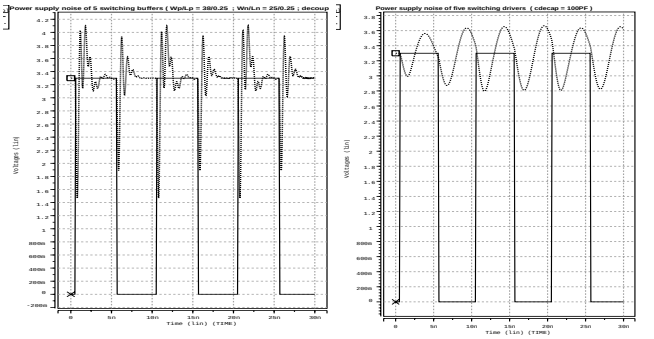

Fig. 2. The power-supply noise for five identical output drivers switching simultaneously. (a) Decoupling capacitor: 2pF (b) Decoupling capacitor: 100pF.

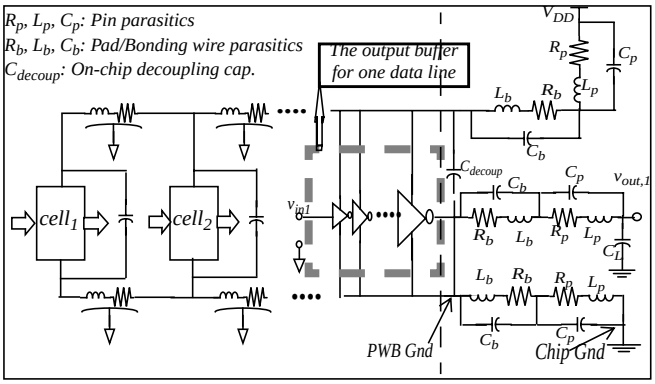

Fig. 3. The circuit schematic for power-supply noise caused by internal and I/O buffer switching.

Fig. 3. shows a circuit model for power supply noise caused by switching in the internal circuitry and the output drivers. The peak amplitude of the supply noise is a function of the number of switching circuits switching simultaneously and the switching activities of the internal circuitry which itself depends on the nature and statistics of the input signals. Power supply noise can thus be modeled as a stochastic process with independent random variables which can in turn be modeled as a Gaussian stochastic process [9]. If one could assume that the switching noise waveforms propagate to the supply lines of the PLL with the same propagation delay regardless of the distance of the switching gates from the PLL and since the decoupling capacitors cannot completely smooth out the spikes from the supply and ground line completely, then the supply noise can be expressed as a train of narrow triangular waveforms with random amplitude which are apart from one another by half the clock period. For the realistic case of different propagation delays, the supply noise is best modeled as a train of trapezoidal waveforms. The pulse width is a random process and is a depends on the number of switching circuits at a single clock period. The pulse width is still small that the power supply noise can be modeled as an impulse train with a uniformly-distributed random shift in $[0,t_r]$.

$$v_n(t) = s(t-\lambda) \qquad \text{where } s(t) = \sum_{n=-\infty}^{\infty} V_{n,max}[n]\delta(t-nT/2)$$

λ is a uniformly-distributed random variable in the interval $[0,t_r]$. t_r is the rise-time of the clock signal. *s(t)* is a periodic waveform having amplitude, $\{V_{n,max}[n]\}$, as a Gaussian random sequence where each sample has the maximum correlation with itself and the correlation with the adjacent samples decays very fast as the time difference between adjacent samples becomes larger. Hence the amplitude can be modeled as a white noise process. We will refer to this as the impulsive supply noise model. It is easily proved that *s(t)* is indeed a wide-sense cyclostationary process[1]. The mean of the process is:

$$\eta_s(t) = \sum_{n=-\infty}^{\infty} E\{V_{n,max}[n]\}\delta\left(t-\frac{nT}{2}\right) \tag{2}$$

and the autocorrelation function:

$$R_s(t_1,t_2) = \sum_{n=-\infty}^{\infty}\sum_{r=-\infty}^{\infty} R_{V_{n,nam}}[n-r]\delta\left(t_1-\frac{nT}{2}\right)\delta\left(t_2-\frac{rT}{2}\right) \tag{3}$$

$E\{.\}$ in Eq. (2) represents the expected value of the random process. Our aim is to determine the statistical properties of the shifted process. It can be proved [9], that the shifted process $v_n(t) = s(t-\lambda)$ is a wide-sense stationary process with mean and autocorrelation as:

$$\eta_{v_n} = \frac{2}{T}\int_0^{T/2}\eta_s(t)dt \qquad ; \qquad R_{v_n}(\tau) = \frac{2}{T}\int_0^{T/2} R_s(t+\tau,t)dt$$

and with the power spectrum as:

$$S_{v_n}(\omega) = \frac{2}{T}S_c(e^{j\omega})|X_{noise}(\omega)|^2$$

By applying the above equations to our special waveforms, the mean, autocorrelation, and the power spectrum of the supply noise can be calculated as follows:

$$\eta_{v_n} = E\{V_{n,max}[n]\}\ ;\ R_{v_n}(\tau) = \frac{\sigma^2_{V_{n,max}}}{t_r}\delta(\tau)\ \ ;\ \ S_{v_n}(\omega) = \frac{\sigma^2_{V_{n,max}}}{t_r} \tag{4}$$

When a large decoupling capacitor is present in the circuit then the supply noise is modeled as a sinusoidal waveform with the random maximum amplitude (c.f. Fig. 2.b.).

$$v_n(t) = V_{n,max}(nT_s)\sin(\omega_n t+\theta) \qquad n\in Z \tag{5}$$

where $T_s = 2\pi/\omega_n$, and $V_{n,max}$ again is a white noise sequence and the random variable Φ is uniform in the interval range $[-\pi,\pi]$ and independent of $V_{n,max}$. We will refer to this as the sinusoidal supply noise model. The oscillation frequency depends on the equivalent switched capacitance, $C_{w,eq}$, the decoupling capacitor, C_d, and the supply and ground inductances, L_v, L_g, and calculated as:

$$f_n = 1/2\pi\sqrt{(L_v+L_g)(C_d+C_{w,eq})} \tag{6}$$

1. Recall that a cyclostationary process is a process whose statistical properties are invariant to a shift of origin by integral multiples of the period (in our case *T/2*).

It is easily proved that $v_n(t)$ is a stationary process possessing the following first and second-order statistics:

$$\eta_{v_n} = 0 \quad ; \quad R_{v_n}(\tau) = \frac{E\{V_{n,max}^2[n]\}}{2}\cos(\omega_n\tau) \quad (7)$$

IV. VCO JITTER ANALYSIS

A voltage-controlled oscillator subject to the supply noise generates waveforms with different frequencies. Therefore even in the lock condition, the noisy VCO can generate frequencies which are different from the input signal frequency. From a system perspective the supply noise is considered as an additive noise source which directly affects the input control voltage. To understand the noise effect of VCO on the PLL loop operation, consider a five stage fully differential ring oscillator-based VCO shown in Fig. 4. [10]. The small fractions next to each transistor shows the gate aspect ratio (*W/L*).

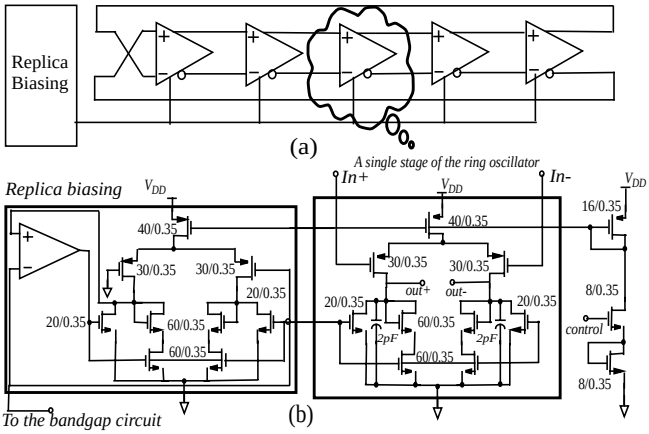

Fig. 4. The VCO based on differential ring oscillator with the voltage controlled resistor and replica biasing. (a) System block diagram (b) Circuit implementation.

This circuit has a good current-frequency linearity[10]. The replica biasing always biases the PMOS transistors such that the voltage swing across each of them is fixed. Under these circumstances, the VCO frequency is a linear function of the bias current source of each delay section [10]. Using the deep submicron BSIM3 MOS model for the transistors, the VCO frequency can be expressed in terms of the input control voltage as follows:

$$f(t) = \frac{kW\upsilon_{sat}C_{ox}}{2NC_{eq}V_{ref}(kW\upsilon_{sat}C_{ox}r_{DS}+1)}(V_{control}-V_{tn}-V_{DS,sat}) \quad (8)$$

The positive-slope, linear *V-f* characteristic obtained from Eq. (8) is justified by the actual *V-f* characteristic of the ring-oscillator of Fig.5. Comparison is provided in Fig. 5. between the actual waveform and the simulated one.

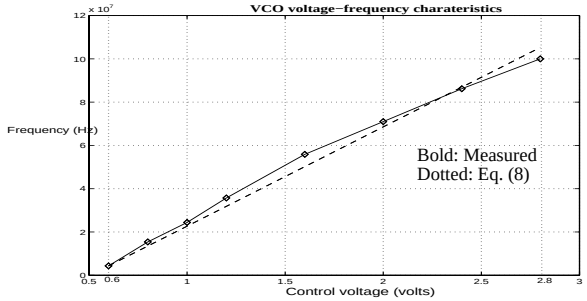

Fig. 5. The voltage-frequency characteristic of the VCO

In light of Eq. (8), the autocorrelation of the excess frequency variation is a linear function of the autocorrelation of the supply noise. Consequently the phase noise of the VCO is obtained for both supply noise models as shown next:

$$S_{\phi_n}(\omega) = \frac{K_{VCO}^2}{\omega^2}S_{v_N}(\omega) = \frac{K_{VCO}^2}{\omega^2}\cdot\frac{\sigma_{V_{n,max}}^2}{t_r} \quad \textit{for impulsive supply noise} \quad (9)$$

$$S_{\phi_n}(\omega) = \frac{\pi K_{VCO}^2}{2\omega^2}(\delta(\omega+\omega_n)+\delta(\omega-\omega_n)) \quad \textit{for sinusoidal supply noise} \quad (10)$$

Taking the inverse Fourier transform gives the autocorrelation as follows:

$$R_{\phi_n}(\tau) = -K_{VCO}^2\cdot\frac{\sigma_{V_{n,max}}^2|\tau|}{t_r} \quad \textit{for impulsive supply noise} \quad (11)$$

$$R_{\phi_n}(\tau) = \left(\frac{K_{VCO}^2}{2\omega_n^2}\cdot\frac{\sigma_{V_{n,max}}^2}{t_r}\right)\cos(\omega_n\tau) \quad \textit{for sinusoidal supply noise} \quad (12)$$

The timing jitter of the VCO is the standard deviation of the timing uncertainty [5], i.e.:

$$\sigma_\tau^2 = \frac{2}{(2\pi f_{clock})^2}(R_{\phi_n}(0)-R_{\phi_n}(\tau)) \quad \textit{for sinusoidal supply noise} \quad (13)$$

Hence the timing jitter for the VCO becomes:

$$\sigma_\tau^2 = \frac{K_{VCO}^2}{2\pi^2 f_{clock}^2}\left(\frac{\sigma_{V_{n,max}}^2|\tau|}{t_r}\right) \quad \textit{for impulsive supply noise} \quad (14)$$

and

$$\sigma_\tau^2 = \frac{K_{VCO}^2}{2\pi^2 f_{clock}^2}(1-\cos(\omega_n\tau)) \quad \textit{for sinusoidal supply noise} \quad (15)$$

V. PLL JITTER ANALYSIS

Due to their desirable features (e.g. not exhibiting any false lock, having a fast acquisition-time, and retaining a zero-phase offset in the lock condition), charge-pump PLLs have found widespread use in frequency synthesizer applications where the signal-to-noise ratios are high. The output voltage of the sequential phase-frequency detector (PFD) can be expressed as a linear function of the phase difference. For the single supply PLL, a DC offset equal is added to the phase-to-voltage mapping function. The output voltage of the PFD acts like a control voltage for the switched current sources of the charge pump circuit. Finally the transfer function of the second-order PLL having a simple RC circuit as the LPF is easily obtained. For the related formulations and derivations see [11]. This familiar formula is presented in Eq. (16) as a reference.

$$H_{PLL}(s) = \frac{\Phi_{out}}{V_N} = \frac{1}{K_{PFD}}\cdot\frac{C_{LP}s}{1+R_{LP}C_{LP}s+(MC_{LP}s^2)/(K_{VCO}K_{PFD})} \quad (16)$$

where

$$K_{VCO} = \frac{kW\upsilon_{sat}C_{ox}}{NC_{eq}V_{ref}(kW\upsilon_{sat}C_{ox}r_{DS}+1)}$$

$$K_{PD} = \left(\frac{I_{CHP}}{2\pi}\right)\left(\frac{1}{\mu_{eff}C_{ox}(W/L)(V_{DD}-V_{th})}\right)$$

Looking at the PLL transfer function reveals that the low frequency component of the phase noise of VCO is attenuated by the closed loop system while the high frequency component of the output follows the variations of the phase noise in VCO. The system of Fig. 1. is linear and the spectral density of the output due to the VCO phase noise is thus obtained using the transfer function of the system.

$$S_{\phi_o}(\omega) = |H_{PLL}(\omega)|^2 S_{\phi_n}(\omega) \quad (17)$$

For a second-order PLL the characteristic polynomial is at least a 4th-order polynomial of ω. To simplify the derivations and obtain a insightful closed-form expression, we assume that the loop filter has a narrow bandwidth. Under this assumption which is valid in most PLL designs, the PLL loop transfer function shows a dominant pole. The effect of the dominant pole decays very fast with

time, and hence the PLL loop transfer function is represented by its non-dominant pole. The power spectrum of output phase is:

$$S_{\phi_o}(\omega) = \left|\frac{1/(RK_{PFD})}{1+(j\omega M)/(RK_{VCO}K_{PFD})}\right|^2 S_{\phi_n}(\omega) \quad (18)$$

The autocorrelation function is:

$$R_{\phi_o}(\tau) = \left(\frac{K_{VCO}^2}{2K_{PFD}} \cdot \frac{\sigma_{V_{n,max}}^2}{s_{p_2}^2 t_r}\right)\exp(-s_{p_2}|\tau|)$$

for impulsive supply noise (19)

$$R_{\phi_o}(\tau) = \left(\frac{K_{VCO}^4}{2\omega_n^2 M^2} \cdot \frac{\sigma_{V_{n,max}}^2}{t_r}\right)\left(\frac{1}{\omega_n^2 + s_{p_2}^2}\right)\cos(\omega_n\tau)$$

for sinusoidal supply noise (20)

The timing jitter of the PLL is obtained as follows:

$$jitter_{\phi_o}(\tau) = \sqrt{\left(\frac{K_{VCO}^2}{2K_{PFD}} \cdot \frac{\sigma_{V_{n,max}}^2}{s_{p_2}^2 t_r}\right)(1-\exp(-s_{p_2}|\tau|))}$$

for impulsive supply noise (21)

$$jitter_{\phi_o}(\tau) = \sqrt{\left(\frac{K_{VCO}^4}{2\omega_n^2 M^2} \cdot \frac{\sigma_{V_{n,max}}^2}{t_r}\right)\left(\frac{1}{\omega_n^2 + s_{p_2}^2}\right)\cos(\omega_n\tau)}$$

for sinusoidal supply noise (22)

s_{p2} in equations (19) and (20) refers to the non-dominant pole of the PLL which equals to:

$$s_{p_2} = -\left(\frac{RK_{VCO}K_{PFD}}{M}\right)$$

VI. Circuit Design and Simulation

A complete PLL clock generator circuit whose structure is similar to the circuit proposed in [10] was designed in 0.35µ CMOS technology. The PLL operates with a lock range from 10MHz up to 250MHz. The phase frequency detector is a conventional sequential phase-frequency detector. The VCO circuit schematic is shown in Fig. 4. The required reference for the replica biasing circuit is provided by a bandgap reference depicted in Fig. 5. This circuit generates a fixed 0.8V and this voltage has 0.9% variation to a temperature variation from $25°C$ up to $145°C$. It also has very robust to supply variation (1% variation for a supply variation from 2.3V to 3.8V. The out put voltage of this bandgap circuit is:

$$V_{ref,bg} = \frac{R_4}{R_2}\left(V_{ref,0} + \frac{R_2}{R_3}V_T\ln(N)\right)$$

where $V_{ref,0}$ s the built-in voltage of the diode and has negative voltage coefficient of -2mV/$°C$. Clearly the output reference voltage can be freely changed from the conventional reference voltage of 1.25V by the ratio R_4/R_2[12].

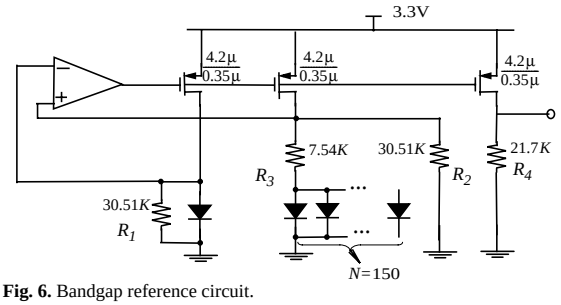

Fig. 6. Bandgap reference circuit.

The experiment setup is shown in Fig. 7. The five inverter are connected to the same voltage and ground lines as the PLL. The drivers switch simultaneously and the jitter of the PLL due the supply noise is measured. Table 1. shows the a comparison of the simulated phase noise levels of PLL with the measured results. Compared to the measurements the results are very closed in frequency range where the VCO phase noise is dominant. This shows the validity of our VCO phase noise formulations.

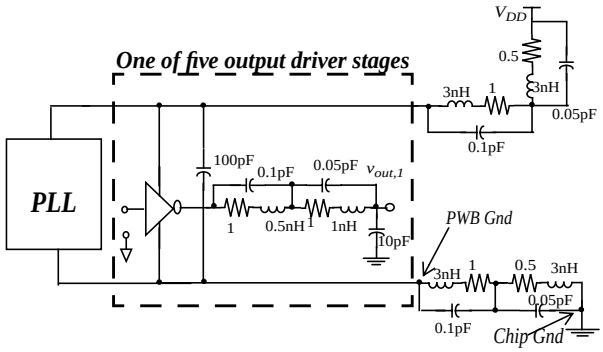

Fig. 7. The expermient setup for measuring the jitter.

Table 1: Comparison between the simulation and the measured results

Frequency offset (kHz)	Simulated jitter [dB/Hz]	measured [dB/Hz]
5.3	-92.2	-93.4
9.1	-96.4	-97.5
15.7	-100.3	-103
32.3	-109.3	-111.2
40	-110	-111.4
64	-112.4	-114.3
80	-115.6	-116.2
100	-119.7	-121.8

VII. Conclusion

This paper presented a mathematical model for calculating the power supply noise induced timing jitter in PLLs. The model relies on the stochastic representation of the supply noise and its effect on the jitter of the VCO and finally the timing jitter of the PLL. Experiments results demonstrate the accuracy of the analytical predictions compared to the measured results.

VIII. References

[1] G. A. Katopis, "Delta-I Noise Specification for a High Performance Computing Machine", *Proc. IEEE*, pp. 1405-1415, Sept. 1985.

[2] R. Senthinathan, J. L. Prince, "Simultaneous Switching Ground Noise Calculation for Packaged CMOS Devices", *IEEE. J. of Solid-State Circuits*, vol. 26, No. 11, pp. 1724-1728, Nov. 1991.

[3] P. Larsson, "di/dt noise in CMOS Integrated Circuits", *Analog Integrated Circuits and Signal Processing*, No. 1.2, pp. 113-130, Sept. 1997.

[4] S. R. Vemuru, "Effects of Simultaneous Switching Noise on the Tapered Buffer Design", *IEEE Trans. VLSI Systems*, vol. 5, no. 3, Sept. 1997.

[5] A. Hajimiri, T. H. Lee, "A General Theory of Phase Noise in Electrical Oscillators", *IEEE I. Solid-State Circuits*, vol. 33, No. 2, Feb. 1998.

[6] A. Demir, A. Mehrotra, J. Roychowdhury, "Phase Noise in Oscillators; A Unifying Theory and Numerical Methods for Characterisation", *ACM/IEEE Design Automation Conference*, June 1998.

[7] F. Herzel, B. Razavi, "Oscillator Jitter Due to Supply and Substrate Noise", *IEEE Custom Integrated Circuit Conference*, pp. 23.6.1-23.6.4, May 1998.

[8] V. F. Kroupa, "Noise Properties of PLL Systems", *IEEE Trans. Comm.*, vol. COM-30, No. 10, pp. 2244-2252, Oct. 1982.

[9]A. Papoulis, *Probability, Random Variables, and Stochastic Processes*, McGraw-Hill Inc., 1991.

[10]I. A. Young, J. K. Geason, K. L. Wong, "A PLL Clock Generator with 5 to 110 MHz of Lock Range for Microprocessors", *IEEE J. Solid-State Circuits*, vol. 27, No. 11, pp. 1599-1607, Nov. 1992.

[11]D. Johns, K. Martin, *Analog Integrated Circuits Design*, John Wiley & Sons, 1997.

[12]H. Banba, H. Shiga, A. Umezawa, T. Miyaba, T. Tanzawa, S. Atsumi, K. Sakui, " A CMOS Bandgap Reference Circuit with Sub-1V Operation", *IEEE J. of Solid-State Circuits*, vol. 34, No. 5, May 1999.