A Single-Chip Dual-Band 22–29-GHz/77–81-GHz BiCMOS Transceiver for Automotive Radars

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***Abstract*—Integration of multi-mode multi-band transceivers on a single chip will enable low-cost millimeter-wave systems for next-generation automotive radar sensors. The first dual-band millimeter-wave transceiver operating in the 22–29-GHz and 77–81-GHz short-range automotive radar bands is designed and implemented in 0.18-μm SiGe BiCMOS technology with $f_T/f_{\max}$ of 200/180 GHz. The transceiver chip includes a dual-band low noise amplifier, a shared downconversion chain, dual-band pulse formers, power amplifiers, a dual-band frequency synthesizer and a high-speed highly-programmable baseband pulse generator. The transceiver achieves 35/31-dB receive gain, 4.5/8-dB double side-band noise figure, >60/30-dB cross-band isolation, −114/−100.4-dBc/Hz phase noise at 1-MHz offset, and 14.5/10.5-dBm transmit power in the 24/79-GHz bands. Radar functionality is also demonstrated using a loopback measurement. The 3.9 × 1.9-mm^2 24/79-GHz transceiver chip consumes 0.51/0.615 W.**

***Index Terms*—Millimeter-wave integrated circuits, automotive radar, pulsed radar, direct-conversion receiver, direct-conversion transmitter, frequency conversion, phase locked loops, frequency synthesizers, injection-locked oscillators, dual-band, 24 GHz, 77 GHz, 79 GHz, pulse generator.**

I. Introduction

RESEARCH and development of silicon-based solutions for millimeter-wave (MMW) applications has gained significant momentum in recent years. These applications include 60-GHz short-range high data-rate communications, automatic cruise control (ACC) and collision-avoidance systems using 24/77-GHz automotive radars, and more recently, 94-GHz security applications using passive imaging.

Automotive radar sensors enable a 360° safety zone around the vehicle. Several short-range sensors are usually mounted around the vehicle to detect objects at close range (0–40 m), which enable collision-avoidance and stop-and-go applications [1]. On the other hand, a single forward-looking sensor may be sufficient for long-range detection (∼150 m), primarily used for ACC. In the last few years, silicon-based 24-GHz short-range automotive radars have been investigated both by industry and academia [1]–[5]. In fact, 24-GHz silicon-based short-range radar sensors have already been deployed in the commercial automotive market [2]. Intensive research and development is also underway for developing 77-GHz long-range and 77–81-GHz short-range radars in silicon technologies [6]–[13]. Highly integrated silicon ICs with sophisticated electronically-steered phased arrays have also been demonstrated both in the K band [14]–[17] and the W band [18], [19]. Most of the current efforts have focused on chip development in high-performance silicon-germanium (SiGe) technologies. A SiGe-based four-channel transceiver (TRX) IC for use in long-range ACC and collision-avoidance systems is in production [7]. Experimental results on a 75-GHz transceiver in 90-nm CMOS have recently been reported by the industry [20].

A clear trend in wireless applications during the last decade has been the push towards higher integration, and multi-mode and multi-band operation, in order to enable low-cost high-functionality consumer devices. As the deployment of silicon-based MMW technology becomes widespread, similar trends may be expected in the MMW space. A dual-band 90-nm CMOS receiver chip, operating in the 60-GHz and 77-GHz bands, was recently reported [21]. Simultaneous operation of a 60-GHz device as a radar and a communication system has been investigated [22]. Furthermore, development of a multi-mode 76-81-GHz silicon-based phased-array transceiver for operation as both short-range and long-range radars has also been proposed [23].

The principal challenge in the development of any MMW multi-band systems, however, will be the efficient generation and processing of signals in different frequencies in the MMW range on a single chip, while maintaining adequate isolation between the different frequency bands. In order to address these challenges, we first developed a fully integrated dual-band frequency synthesizer for operation in the 24-GHz and 77-GHz radar bands, as demonstrated in [24] and [25]. In continuation of that work, in this paper, we present a highly-integrated MMW pulsed-radar transceiver operating in the 22–29-GHz and 77–81-GHz short-range automotive radar bands. The IC has been implemented in a 0.18-μm BiCMOS technology ($f_T/f_{\max}$ = 200/180 GHz) and was first reported by the authors in [3]. Together, the synthesizer and transceiver ICs represent the first reported attempt towards implementation of highly-integrated dual-band systems in the MMW regime, particularly for automotive radar applications.

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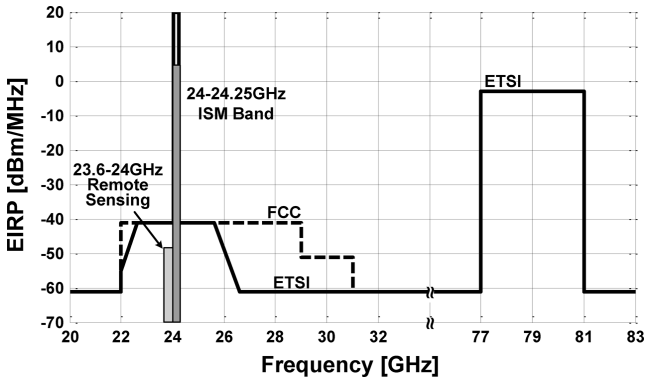

Fig. 1. Spectrum allocations for short-range automotive radars.

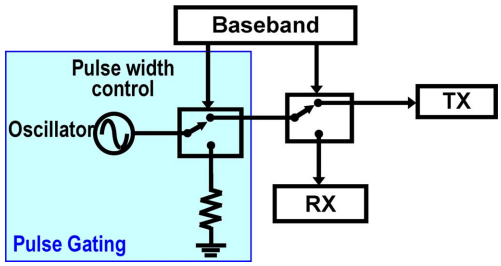

Fig. 2. Conceptual operation of pulsed radar [1].

The remainder of this paper is organized as follows. Section II briefly discusses the various spectrum allocations for automotive radar applications as a motivation of this work. Dual-band transceiver architecture and radar system-level considerations are described in Section III. The design and analysis of the constituent circuits and sub-systems of the transceiver are explained in Section IV. Measurement results of an experimental synthesizer prototype are presented in Section V. Finally, Section VI provides concluding remarks and suggestions for future research.

II. Automotive Radar Spectra

Spectrum regulatory agencies worldwide have allocated several frequency bands exclusively for automotive radar applications. Fig. 1 shows the spectrum allocations, in United States and Europe, for the various systems that operate in the 22–29-GHz and 77–81-GHz bands, including, in particular, the short range automotive radars. The above bands will hereafter be referred to as 24 GHz (or K band) and 79 GHz (or W band), for brevity.

The Federal Communications Commission (FCC) in USA has allocated an unlicensed 7-GHz-wide spectrum between 22–29 GHz with strict emission restrictions [26] (cf. Fig. 1). Similarly, the European Telecommunications Standards Institute (ETSI) has allocated the 22–26-GHz band for short-range automotive radars. As is clear from Fig. 1, both FCC and ETSI allocations overlap with existing systems around 24 GHz. These systems include the unlicensed 24.125-GHz ISM (industrial, scientific, and medical) applications and more importantly, sensitive remote sensing and astronomy equipment [27]. While the FCC stipulates a transmitter center frequency above 24.075 GHz with limited emissions in the 23.6–24.0-GHz band in order to strongly minimize interference with remote sensing and radio astronomy equipment, the ETSI allocation is situated exactly at the center of the aforementioned sensitive applications.

To address the above issue, the ETSI will discontinue the use of the 24-GHz allocation for automotive short-range sensors in mid-2013 [28], thereafter mandating a shift to 79 GHz. While this has spurred the interest in and the development of 79-GHz radar sensors, the mature 24-GHz technology will likely continue to dominate the non-European markets. In fact, no corresponding 79-GHz allocation has yet been made available by the FCC. Therefore, next-generation radar sensors may well be required to support both frequency bands, for compatibility with frequency bands in the rest of the world and for lower overall cost. For this reason, the wideband 22-to-29-GHz and 77-to-81-GHz short-range automotive radar bands have been chosen for the dual-band radar implementation in this work. As will be illustrated in detail in Sections III and IV, several novel circuit techniques are used to achieve dual-band operation, enabling a small die area and low power consumption.

The K-band allocations enable high range resolution due to the high instantaneous bandwidth (4–7 GHz), but restrict the transmitted power levels thereby limiting the maximum achievable range. As discussed in [29], pulses as short as 200 ps (unmodulated) are needed to occupy the available FCC bandwidth of 22–29 GHz. Due to the relatively smaller bandwidth, longer pulses are necessary for the 77–81-GHz band. The rate at which the pulses are sent is called the pulse repetition frequency (prf) and is given by

$$\text{prf} = \frac{c}{2R} \tag{1}$$

where c is the speed of light and R is the minimum unambiguous radar range. Using (1), a minimum unambiguous radar range of 40 m results in a prf of 3.75 MHz. It is important to note that in order to meet the FCC average power emission requirements, either the prf or the pulse power must be decreased. A longer pulse can be transmitted with higher total pulse energy, resulting in a higher SNR. This would require a reduction in prf and the use of pulse compression techniques (e.g., BPSK and PN-coding) [30], in order to meet the spectral limitations and to achieve the same range resolution as a short pulse. Nevertheless, the pulsewidth cannot be arbitrarily increased due to the peak power emission restrictions.

Next, the architecture and system-level considerations of the dual-band transceiver are described.

III. Dual-Band Transceiver Architecture

The proposed dual-band transceiver is based on a pulsed-radar architecture [1], [29]. This architecture is promising for short-range radars as the transmitter and receiver operate in a time-duplexed fashion, thereby achieving a better dynamic range than other radar architectures such as FM-CW and PN-coded radars. The operation of a pulsed

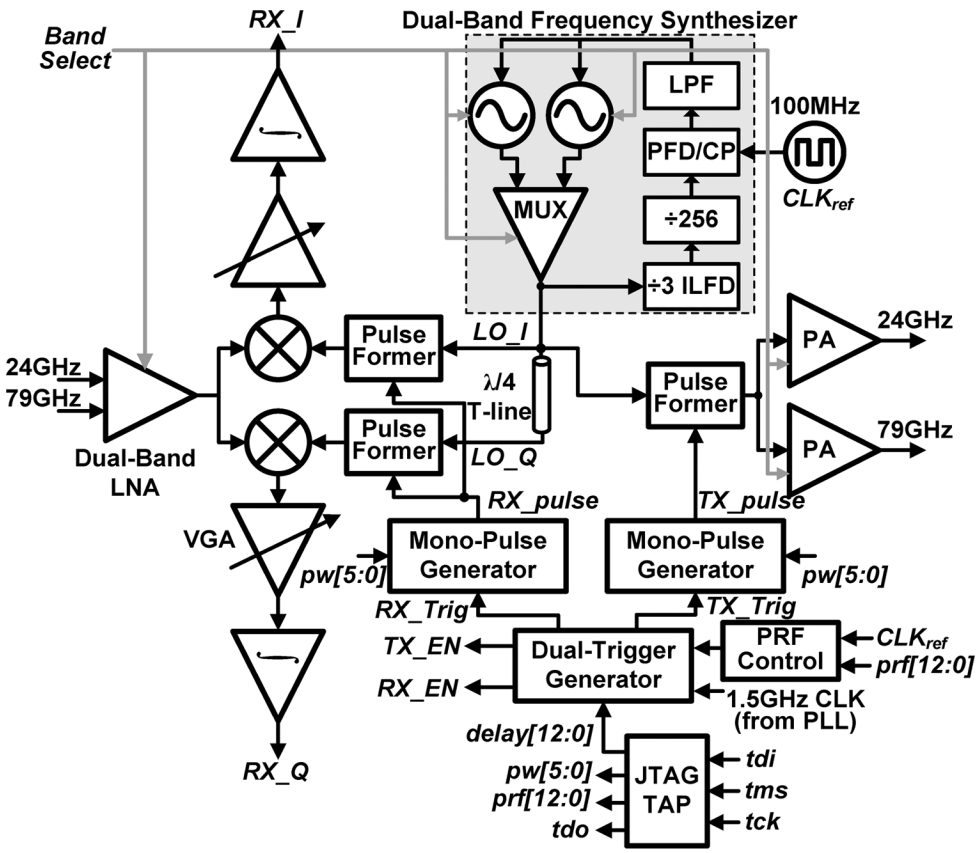

Fig. 3. Block diagram of the 24/79-GHz dual-band transceiver.

radar is conceptually shown in Fig. 2. A baseband pulse is upconverted to the carrier frequency and is transmitted by the sensor at a rate determined by the prf. The reflected pulse from the target is correlated with a locally delayed version of the transmitted pulse in the receiver. The target range is estimated by determining the delay between the instants of pulse transmission and receiver correlation. The interested reader is referred to [1], [29] for operation principles of the pulsed-radar architecture.

Fig. 3 shows the detailed block diagram of the dual-band TRX. The chip is comprised of a receiver (RX), a transmitter (TX), a dual-band frequency synthesizer and a high-speed CMOS pulse generator. Design efforts have been focused on maximizing the re-use of circuits in the two bands to reduce die area. As a result, the downconversion chain in the receiver, the divider chain in the synthesizer, the pulse formers, and the pulse generator are all shared between the two bands, resulting in a lower overall chip area. This design is the first demonstration of a W-band synthesizer integrated within a transceiver, and also is the first reported integration of high speed CMOS digital circuitry with a 24/79-GHz automotive radar transceiver.

In the following discussion, we calculate the radar signal-to-noise ratio, given the typical requirement of detecting a 1-m^2 cross section target at a 40-m range. For the 22–29-GHz FCC allocation, the peak EIRP (Effective Isotropically Radiated Power) must be less than 0 dBm in a 50-MHz bandwidth around the center frequency. This is equivalent to an EIRP of -17 dBm/MHz. For simplicity, we assume that this EIRP density is distributed uniformly across the 7-GHz bandwidth (this is optimistic, but sets the theoretical limit on the achievable performance; this also provides us with the worst-case transmitter output power.). Note that [1] makes the same assumption. This gives us the maximum peak EIRP of

$$\mathrm{EIRP}_{\mathrm{pk}} = -17 + 10 \cdot \log 7000 = 21.5\ \mathrm{dBm}. \tag{2}$$

Receiver antenna gain is calculated as [30]

$$G_{\mathrm{RX}} = \frac{\pi^2}{\theta_e \theta_a} = 15.6\ \mathrm{dBi} \tag{3}$$

where $\theta_e = 15^\circ$ and $\theta_a = 60^\circ$ are the elevation and azimuth half-power beamwidths in radians, respectively, and are typical values for short-range automotive radars.

Radar range equation can be written as

$$R_{\max}^4 = \frac{\mathrm{EIRP}_{\mathrm{pk}} \cdot G_{\mathrm{RX}} \cdot \lambda^2 \cdot \sigma}{(4\pi)^3 kTBF(\mathrm{SNR}_{\min})} \tag{4}$$

where $R_{\max}$ is the radar range, λ is the signal wavelength, σ is the target cross-section, kT is the thermal noise power, B is the receiver noise bandwidth, F is the receiver noise factor and $(\mathrm{SNR}_o)_{\min}$ is the minimum required output signal-to-noise ratio. The required SNR is estimated to be about 11 dB, from the required probability of detection and probability of false alarm

TABLE I
RADAR SYSTEM-LEVEL SPECIFICATIONS

Range=40m, Target cross-section=1m^2, Probability of detection=0.9, Probability of false alarm=10^{-3}			
Frequency Range	**22-29 GHz**	**77-81 GHz**[a]	**77-81 GHz**[b]
Transmit peak EIRP	21.5 dBm	55 dBm	26.1 dBm
Receiver Antenna Gain	15.6 dBi	15.6 dBi	15.6 dBi
Signal Bandwidth	7 GHz	4 GHz	4 GHz
RX Noise Figure[c]	4.5 dB	8 dB	8 dB
Required SNR	11 dB	11 dB	11 dB
Single-pulse SNR	1.1 dB	24.9 dB	−1.2 dB
Number of integrated pulses	10	1	17

[a]Assuming maximum allowable EIRP by ETSI.
[b]Assuming maximum EIRP based on measured results from our transmitter (=10.5+15.6).
[c]Based on receiver measurements.

[31]. From (4), the single-pulse SNR is 1.1 dB, assuming a receiver noise figure of 4.5 dB based on the measured results of the 24-GHz receiver. It is clear that multiple received pulses must be integrated in order to improve the SNR and to raise the signal above the noise floor; coherent integration of n pulses ideally results in an n-fold improvement in SNR. Coherent integration of 10 pulses is sufficient in this case to meet the required SNR target of 11 dB. In practice, more pulses would need to be integrated to ensure sufficient link margin.

For the 77–81-GHz band, ETSI has stipulated a generous 55-dBm peak EIRP limit. Following the same procedure as for the 22–29-GHz band above, we obtain a single-pulse SNR of about 25 dB assuming 8 dB noise figure, obviating the need to integrate multiple pulses. Nevertheless, in current silicon technologies, such power levels are difficult, if not impossible, to achieve. Using the measured transmitter output power of 10.5 dBm in the radar range equation and assuming the same transmit antenna gain as that of the receive antenna, we obtain a single-pulse SNR of -1.2 dB. In order to meet the SNR requirements, at least 17 pulses must be integrated. The above results are summarized in Table I.

IV. TRANSCEIVER IMPLEMENTATION

A. Receiver

The receiver in Fig. 3 consists of a dual-band LNA (DB-LNA), I/Q broadband downconversion mixers, I/Q dual-band pulse-formers, and variable-gain baseband amplifiers and integrators. The design of the receiver pulse-formers is similar to that of the transmitter pulse-former, and is discussed in detail in Section IV.B. As mentioned before, the entire downconversion chain (i.e., following the LNA) is shared between the two bands, resulting in a simple architecture and reduced die area.

The key circuit that enables dual-band operation in the receiver is the DB-LNA. As shown in the circuit schematic of Fig. 4(a), the DB-LNA has two inputs, RF_{24} and RF_{79}, corresponding to the two frequency bands, and a single multiplexed output, $\mathrm{RF}_{\mathrm{OUT}}$. A two-stage cascode LNA with inductive degeneration is used for each band. The outputs of the second stages in the two paths are combined into a dual-band passive network comprising of the center-tapped inductor L_3 (0.2 nH), the capacitors C_3–C_4 (0.2 pF) and the t-lines T_3–T_4 (0.1 nH), thereby resulting in a single output for both bands. Only one of the paths is active at a time; while the unused path is turned off.

In the 79-GHz path, emitter degeneration is implemented by short-circuited t-lines T_{12} (20 pH) and T_{14} (10 pH). T_{12} and T_{14} include the parasitic inductances of the vias—with approximately 3-pH value based on EM simulations—to the HBT emitters. The input pad, the DC blocking MIM capacitor C_{11} (0.2 pF) and the series t-line T_{11} (25 pH) are part of the input matching network. Inter-stage matching network is composed of T_{13} (125 pH) and C_{12} (0.2 pF). Similarly, the 24-GHz path includes degeneration inductances T_{22} and T_{24} (both 50 pH) for input matching and stability, respectively. The series inductance L_{21} (0.2 nH) and first-stage load L_{23} (0.29 nH) are implemented as spiral inductors. MIM capacitors C_{21} and C_{22} (both 0.2 pF) are used for inter-stage AC coupling. The core of the dual-band load at the outputs of the two LNAs is formed by the center-tapped spiral inductor L_3 (0.2 nH) and capacitors C_3–C_4 (0.2 pF). The outputs of the two paths are connected to this dual-band core through the t-lines T_3–T_4, as shown in the DB-LNA die micrograph of Fig. 4(b). These interconnects are necessitated by the arrangement of the input/output pads, which itself is restricted by probing requirements. In Fig. 4(b), additional t-line segments can be observed within the dual-band load and between the dual-band load and GSG pads. Although not explicitly shown in Fig. 4(a), these passives are taken into account in the EM simulations during the design of the dual-band network.

The dual-band operation of the LNA output matching network arises from the mutual coupling of the center-tapped inductor. This is shown in Fig. 5, where the dual-band core is redrawn along with its equivalent circuit. The center-tapped inductor, 2 L, is replaced by a T-network consisting of two inductors of value $(1-k)L$ and a third inductor of value kL, where k is the magnetic coupling factor between the two coils of the center-tapped spiral inductor ($k = 0.4$ for inductor L_3). The series combination of kL and C_1 results in a series resonance which provides the notch between the two bands. A plot of the driving-point impedance, Z_{in}, of this multi-order equivalent circuit as a function of frequency is shown in Fig. 5, clearly indicating two resonant frequencies.

The straightforward operation described above is complicated by the presence of other passive components that result due to unavoidable interconnects (such as T_3 and T_4) and

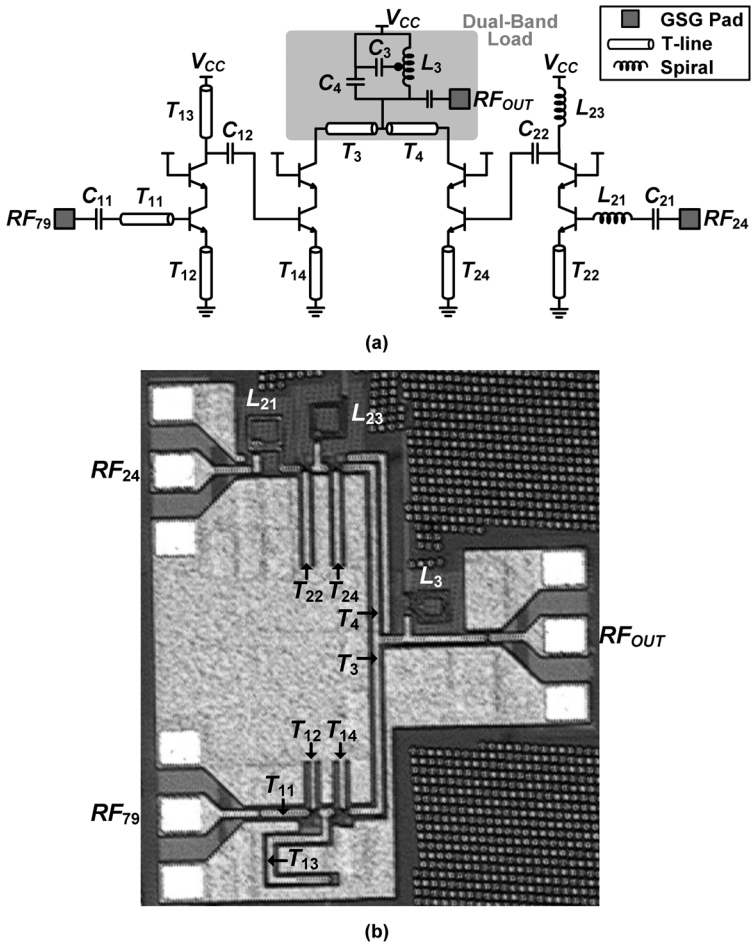

Fig. 4. (a) Simplified schematic of the dual-band LNA. (b) Die micrograph of the DBLNA indicating constituent t-lines and spirals.

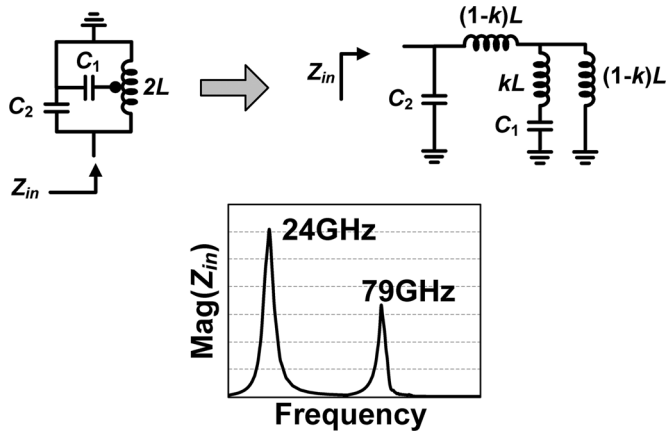

Fig. 5. Equivalent circuit and driving-point impedance of the dual-band load.

loading from the mixer input. T_3–T_4 have negligible effect on the performance in the K-band as their resonances with the HBT output capacitances occur beyond 100 GHz. The most critical loading is that due to the mixer input capacitance. Moreover, the design elements L, C_1, C_2, and k are in general frequency-dependent and therefore several iterations are necessary to obtain the desired circuit performance. First, the output impedances of the second cascode stages are obtained from simulations. These can be expressed as series *RC* networks as shown in Fig. 6. The real part varies from 25 Ω to 36 Ω between the two bands, while the capacitance is relatively constant at 15 fF. Similarly, the mixer input impedance is found as a series combination of 30 Ω and 70 fF and is connected to the output of the dual-band network. Now, the reactive impedances of the input and output terminations can be treated as part of the dual-band network design, as depicted in Fig. 6. The dual-band network is optimized for low loss in the 79-GHz band at the expense of some performance in the 24-GHz band, which is easily compensated by the high device gain in the K band. The resultant S-parameters of the network are shown in Fig. 6. The dual-band network achieves an insertion loss of 1.4–3.5 dB in the 22–29-GHz band and 1–1.1 dB in the 77–81-GHz band. Note that the input and output of the dual-band network in Fig. 6 show moderate match in the 79-GHz and 24-GHz bands, respectively. This shows that some performance is sacrificed in order to obtain dual-band operation. Nevertheless, the degradation in insertion loss is on the order of only a few tenths of dB, as inferred from simulations.

Tapered coplanar GSG pads are used for better modeling accuracy [32] and are absorbed in the matching network design. All t-lines are implemented as conductor-backed coplanar waveguide structures [33]. The DB-LNA circuit occupies 0.75×0.65-mm^2 including the GSG pads.

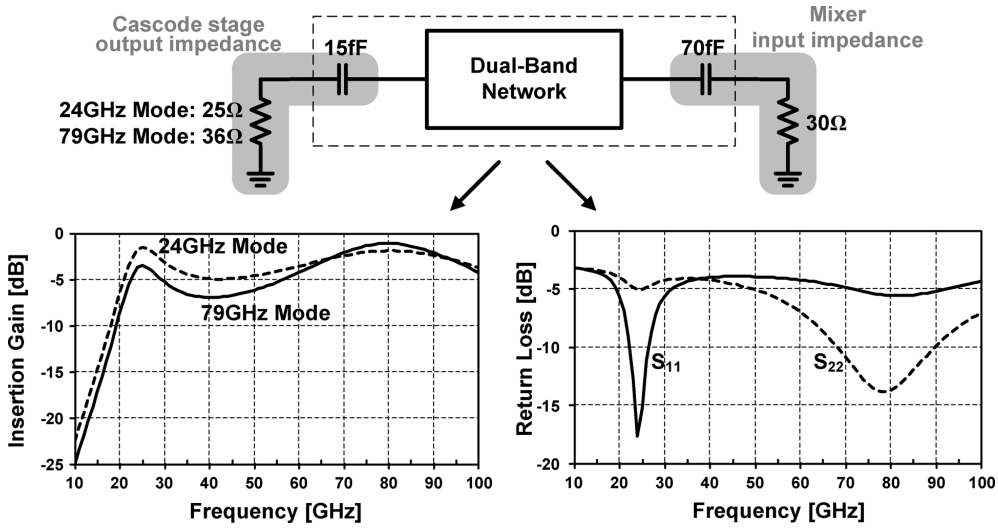

Fig. 6. Simulated S-parameters of the dual-band matching network terminated with the output impedance of the cascode stage and the input impedance of the mixer.

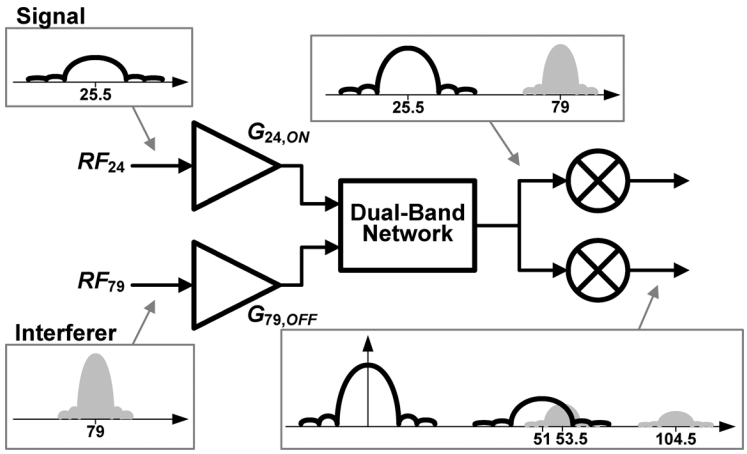

Fig. 7. Signal spectra along the receiver chain in the presence of an interferer in one of the paths.

A critical challenge in any single-chip multi-band system is to achieve sufficient isolation among the bands. Most implementations solve this problem by employing completely separate RF chains for different bands. In this work, the outputs of the LNAs in the two bands are multiplexed into a single output, resulting in high cross-band isolation requirements. Although only one path is active at a time, an interferer from the other input can desensitize the following mixer. In order to understand the need for isolation, consider the LNA-mixer block diagram of Fig. 7. In this example, the desired signal is centered at 25.5 GHz and an interferer appears at the 79-GHz input. Accordingly, the 24-GHz path is enabled while the 79-GHz path is turned off. Consequently, the 24-GHz LNA provides an on-state insertion gain of $G_{24,\mathrm{ON}}$ to the desired signal while the 79-GHz interferer experiences an off-state attenuation of $G_{79,\mathrm{OFF}}$. The LO signals of the downconversion mixers are in the 24-GHz band. The 24-GHz input signal is downconverted to DC by the mixer while also generating the sum frequency component at 51 GHz. The 79-GHz signal also results in two outputs, one at 53.5 GHz and the other at 104.5 GHz. Except the desired output at DC, all other mixing products are filtered in the low-pass baseband circuitry. Thus, the interferer does not result in in-band frequency components at the mixer output (ideally, at least). Nevertheless, if the interferer power level at the mixer input is higher than the input $\mathrm{P}_{1\mathrm{dB}}$ (1-dB compression point) of the mixer, it will result in circuit non-linearities in the signal band, affecting the detection of the desired signal [34]. The above statements hold true for the other case as well, i.e., when the desired signal is in the 79-GHz band and the interferer in the 24-GHz band. Therefore, high isolation is necessary from each input to the LNA output in the off-state. To this end, a dedicated first stage is used in each path, and cascode topology is used for the amplifier stages. Furthermore, series T-lines T_3–T_4 improve isolation between the two paths by partially resonating out the parasitic capacitances at the collector terminals of the second-stage cascode transistors which, in turn, results in an increase in the amplifier's gain.

The LNA is followed by double-balanced I/Q mixers, variable gain amplifiers (VGAs) and integrators. The I/Q mixers are Gilbert-cell mixers with resistive degeneration for input matching. As discussed earlier, the dual-band matching network provides power match between the LNA output and the mixer input. As observed from Fig. 6, the power match is better

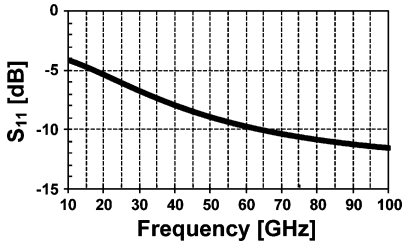

Fig. 8. Simulated input return loss of the mixer.

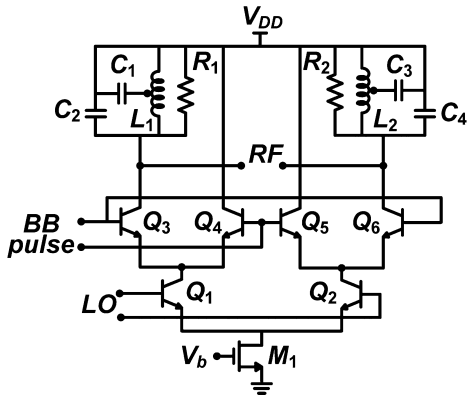

Fig. 9. Schematic of the dual-band pulse former circuit.

than −10 dB in the 79-GHz band and is around −5 dB in the 24-GHz band. Simulations of the standalone mixer (i.e., without the dual-band network), shown in Fig. 8, also reveal broadband input return loss better than −5 dB in the 24-GHz band and −10 dB in the 79-GHz band. Due to abundant HBT gain in the 24-GHz band, the relatively poor return loss is readily accommodated. Pulse formers generate the reference pulses for correlation with the received pulses in the mixers. The VGAs are also implemented as a Gilbert-cell topology, where their gains are controlled by the bias current. The integrate-and-dump circuitry is a G_m-C based design, similar to the one reported in [2].

B. Transmitter

The transmitter consists of a dual-band pulse former, and 24-GHz and 79-GHz wideband power amplifiers (PAs). The signal flow in the transmitter is the inverse of that in the receiver, except for the absence of quadrature signals. As shown in Fig. 3, the pulse former is shared between the 24-GHz and 79-GHz paths and its dual-band output drives the two PAs. The PAs provide separate outputs for the two radar bands.

Fig. 9 illustrates the dual-band pulse-former circuit, which is essentially a double-balanced Gilbert-type upconversion mixer with dual-band *LC* tank outputs, enabling it to upconvert the baseband pulse to the transmitter carrier frequency in either of the two bands. The Gilbert cell is formed by the current-steering quad Q_3–Q_6 stacked on top of the lower differential pair Q_1–Q_2. An nMOS tail current source M_1 provides the bias current of the pulse former. The dual-band output loads have the same topology as the dual-band network used in the LNA. They consist of center-tapped spiral inductors L_1–L_2 (200 pH), MIM capacitors C_1–C_4 (200 fF) and load resistors R_1–R_2 (100 Ω). The dual-band network increases the conversion gain of the mixer and provides bandpass filtering in the 24-GHz and 79-GHz bands to restrict the transmitted signal within the regulated transmit mask. LO leakage is reduced by terminating one of the differential pair outputs in an AC short circuit, so that the mixer quad steers the output currents into the supply when the baseband pulse is in the off-state. The baseband pulse inputs are applied to the mixer quad Q_3–Q_6 and the LO inputs to the lower differential pair Q_1–Q_2. This configuration, combined with the inherent benefits of the double-balanced topology, further reduces the LO leakage to the transmitter output [8]. The pulse former is followed by emitter follower buffers to drive the two PAs. The input pads of the PAs, included for debugging purposes, are absorbed into the buffer design and can be removed in a revised implementation for improved performance.

The schematics of the 79-GHz and 24-GHz transmitter PAs are shown in Fig. 10(a) and (b), respectively. Both PAs consist of common-emitter stages operating in Class-A mode. The 79-GHz PA is a cascade of three single-ended common-emitter HBT amplifier stages. The first and second stages each consists of two 10.16-μm-long HBT devices $(Q_3$–$Q_4)$ in parallel, while the third stage consists of four parallel HBTs (Q_5) in order to achieve higher output power. Due to the higher device gain in the 24-GHz band, only two stages are needed for the 24-GHz PA. The HBTs Q_6 $(2 \times 10.16\ \mu\text{m})$ and Q_7 $(4 \times 10.16\ \mu\text{m})$ are sized similar to the devices in the 79-GHz PA. A cascode pre-driver, consisting of the HBTs Q_1–Q_2 $(2 \times 10.16\ \mu\text{m})$, precedes the three-stage 79-GHz PA to provide additional signal amplification, while also improving the LO feedthrough and the isolation between the two transmit paths. The PAs operate from a 1.8-V supply as the BV_{CEO} of the high-speed HBTs in this process is 1.9 V. The bias networks of the amplifier stages are designed to provide a base impedance of about 200 Ω. This impedance corresponds to a BV_{CER} of 3.5 V, which is high enough to prevent HBT breakdown at the intended PA output power levels in this work. 0.2-pF and 1-pF MIM capacitors are used for inter-stage AC coupling in the 79-GHz and 24-GHz PAs, respectively. Input, output and inter-stage matching networks are designed using t-lines and MIM capacitors. The t-lines are implemented as conductor-backed coplanar waveguide (CPW) structures. The GSG pads are absorbed in the input and output matching networks.

The design of the PAs was carried out with the aim of first-pass success, at the expense of some performance. Most importantly, the 24-GHz PA incorporates t-line-based matching networks instead of spiral inductors to ensure modeling accuracy, as t-lines provide well-defined return current paths. T-lines with characteristic impedance Z_0 of only 46 Ω are used in the design, with the exception of the shunt stubs in the single-stub tuned matching networks at the inputs of all stages in the 79-GHz PA. T-lines with a Z_0 of 74 Ω and an electrical length of 94° are used to implement these shunt stubs, which also feed the DC bias to the HBT inputs. The electrical lengths of the 46- Ω t-lines vary from 14° to 42° in the 79 GHz PA, and from 14° to 25° in the 24-GHz PA. The quarter-wavelengths of the 46- Ω lines are

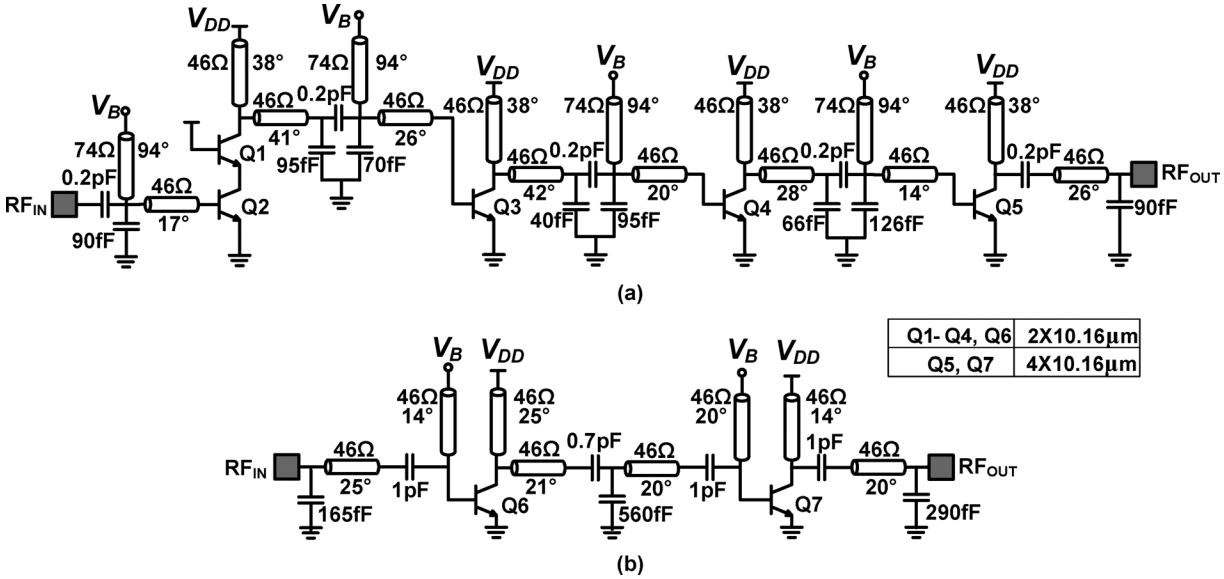

Fig. 10. Schematics of (a) the 79-GHz and (b) the 24-GHz power amplifiers.

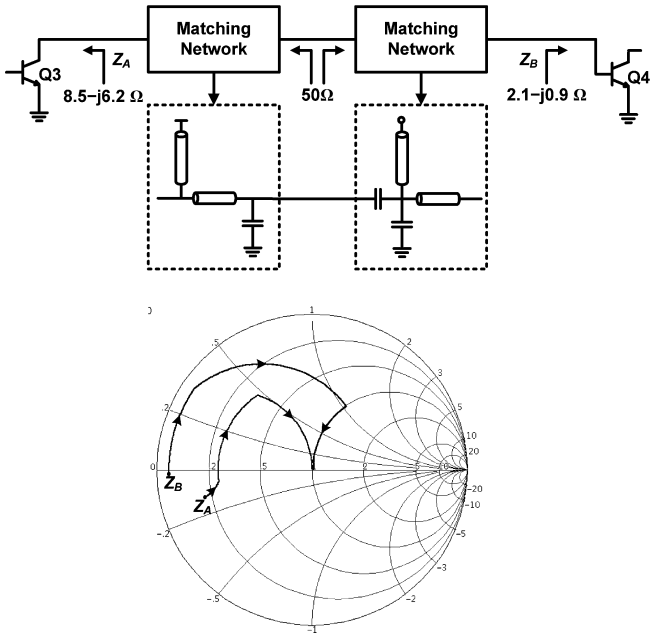

Fig. 11. Inter-stage matching methodology in the PAs.

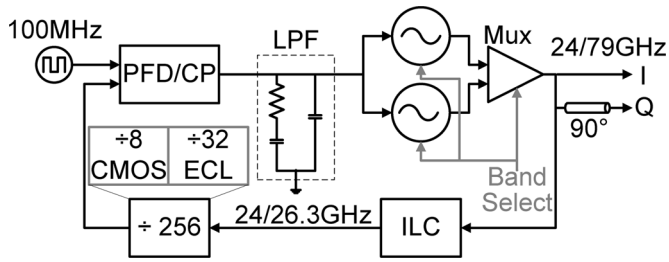

Fig. 12. Block diagram of the dual-band frequency synthesizer.

about 425 μm and 1.5 mm in the 79-GHz and 24-GHz bands, respectively.

In order to design the inter-stage matching networks, the output impedance of the preceding stage and the input impedance of the following stage are determined. At this point, a matching network can be readily synthesized to directly match the aforementioned impedances. But, in this work, a different approach has been adopted. The methodology for the design of matching networks is illustrated in Fig. 11, taking the matching network between the second and third stages of the 79-GHz PA as an example. The output impedance of the second stage transistor, Q_3, is $Z_A = 8.5 - \mathrm{j}6.2\ \Omega$, while the input impedance of the third stage HBT, Q_4, is depicted as $Z_B = 2.1 - \mathrm{j}0.9\ \Omega$. Individual matching networks are designed to transform each of these impedances Z_A and Z_B to 50 Ω, as shown graphically on the Smith chart of Fig. 11. The resulting networks are then directly cascaded to accomplish inter-stage matching. While this approach results in more elements in the inter-stage matching networks and hence higher insertion loss of the matching networks, it enables easy and straightforward design. Each stage can be designed individually using this approach as its input/output matching networks are not affected by the terminal impedances of the preceding and following stages. This is especially beneficial in the PA design in this work as the power HBTs have significant feedforward capacitance and the output matching network affects the input impedance of each amplifier stage.

C. Dual-Band Frequency Synthesizer

The transceiver chip includes a dual-band frequency synthesizer which provides the sinusoidal carriers for upconversion of the baseband pulses to the 24-GHz and 79-GHz bands. The block diagram of the synthesizer is shown in Fig. 12. The design is an improved variant of the 24/77-GHz synthesizer chip reported in [24], [25]. The synthesizer consists of two VCOs, one for each radar band. The outputs of the VCOs are multiplexed into the input of an injection-locked circuit (ILC). The ILC acts as a divide-by-three circuit for the 79-GHz input and as a tuned

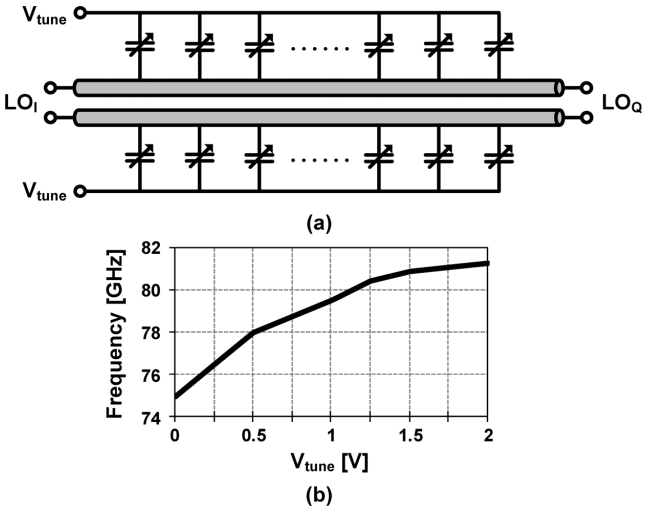

Fig. 13. (a) Dual-band quadrature LO generation using quarter-wave coupled lines. (b) Simulated frequency at which the coupled lines are 3 $\lambda/4$ long, as a function of the varactor tuning voltage.

buffer for the 24-GHz input. Thus, the division ratio is 768 in the 79-GHz band and 256 in the 24-GHz band. Static emitter-coupled logic (ECL) and CMOS dividers, CMOS phase-frequency detector, charge-pump and an off-chip low-pass filter close the loop and lock the synthesizer output to a 100-MHz crystal reference signal. Note that only one of the VCOs is operating at a time. Design, analyses and measurements of the synthesizer circuits are discussed in depth in [25]. Only key additions and improvements over the original design are discussed here. Specific improvements include precise prediction of the operation frequency through a more accurate inductor model, as described in [25], and quadrature generation required for direct downconversion. Furthermore, the W-band VCO tuning range has been shifted to span the 77–81-GHz band.

The 79-GHz VCO is a modified differential Colpitts oscillator, with an *LC* degeneration technique which enables higher oscillation frequencies, higher tuning range and lower phase noise compared with other topologies [25]. The 24-GHz VCO is a cross-coupled *LC* oscillator design with the tank formed by a spiral inductor and MOS varactors. The 24-GHz and 79-GHz VCO cores draw 4 mA and 10 mA, respectively, from a 2.5-V supply. The injection-locked circuit enables seamless reconfiguration of the division ratio between the two bands of the frequency synthesizer. The ILC can lock to input signals in a wide frequency range of 68.7 GHz to 85 GHz [25]. The ILC draws 2 mA and 6 mA from a 2.5-V supply in the 24-GHz and 79-GHz bands, respectively. Details of the ILC design and operation can be found in [25] and [35].

An important addition in the synthesizer over the design in [25] is the generation of quadrature outputs. In this work, the dual-band quadrature signal is generated through varactor-loaded quarter-wave coupled transmission lines, depicted in Fig. 13(a). In order to understand the circuit operation, consider a low-loss transmission line of length l. The phase shift introduced by the line is given by

$$\Delta\phi = \frac{2\pi l}{\lambda} \tag{5}$$

where λ is the line wavelength. If a line has a length $l_1 = \lambda_1/4$ at a frequency f_1 in the 24-GHz band, the phase-shift of the line at f_1 can be calculated from (5) as

$$\Delta\phi@f_1 = \frac{2\pi}{\lambda_1}\cdot\frac{\lambda_1}{4} = \frac{\pi}{2} \tag{6}$$

indicating a phase-shift of 90°. The phase-shift at the frequency 3 f_1 can be similarly written as

$$\Delta\phi@3f_1 = \frac{2\pi}{\lambda_1/3}\cdot\frac{\lambda_1}{4} = \frac{3\pi}{2} \tag{7}$$

indicating a phase-shift of 270° or equivalently $-90°$. Therefore, a quarter-wave t-line in the 24-GHz band can provide 90° phase shift in the 24-GHz band and $-90°$ in the 79-GHz band. Such a t-line can then be used to generate a signal in quadrature with the LO signal from the frequency synthesizer in both bands (the sign of the phase shift is inconsequential in the signal downconversion). As shown in Fig. 13(a), quarter-wave coupled lines (for differential signals) are used to generate LO_Q, which is in quadrature with the synthesizer output LO_I. Since a quarter-wave line provides 90° phase-shift only at a certain frequency, a tuning mechanism is necessary to cover the tuning range of the VCOs. Therefore, the coupled lines are periodically loaded with MOS varactors that fine tune the electrical length of the lines to $\lambda/4$. With the introduction of MOS varactors, the passive structure of Fig. 13(a) can be considered as a loaded line phase shifter [36]. Each of the varactors contributes a tunable phase-shift given by

$$\Delta\phi_{\mathrm{var}} = \tan^{-1}[\pi f Z_0 C(V)] \tag{8}$$

where Z_0 is the characteristic impedance of the line and $C(V)$ is the variable capacitance of the varactors. The coupled lines are laid out with side and bottom ground shields, and holes are made in the bottom ground plane where the lines connect to the varactors. Fig. 13(b) shows the simulation plot of the frequency at which the phase-shifter provides a quadrature phase shift in the 79-GHz band, as a function of the varactor tuning voltage V_{tune}. The entire 79-GHz band is readily covered using the aforementioned tuning mechanism. The simulated I/Q mismatch is better than 2°. While the additional phase shift from the varactor helps reduce the line length, it also introduces loss due to signal reflection from the varactor load. Furthermore, varactors inherently add loss due to finite Q, especially in the 79-GHz band. The LO buffers are designed to provide sufficiently high voltage swings at the inputs of the pulse formers so that their conversion gain is insensitive to the frequency-dependent losses in the 90° phase-shifter network. Note that the phase-shift in (8) is not linear with frequency, resulting in a dispersive line. This effect is further exacerbated by the non-linear tuning curve of the varactors. In spite of the above drawbacks, a directional coupler or a more complex I/Q generation circuitry was not employed, in order to obtain first-pass success.

D. Baseband Pulse-Generator

Several pulse generator designs have been reported in prior art [4], [37]. A CMOS pulse generator, generating pulses directly in the 22–29-GHz band, was reported in [37]. The design

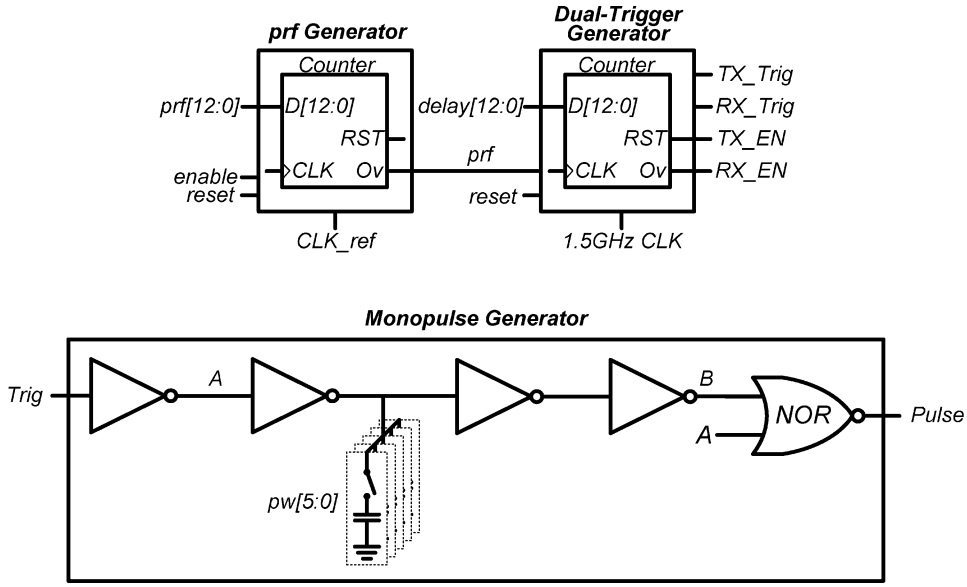

Fig. 14. Pulse generator schematics.

required precise transistor dimensions for predicting the center frequency of the pulse accurately, and no method for controlling and programming the pulsewidth was reported. The pulse generator in this work has been designed using CMOS logic requiring no DC power consumption. The CMOS implementation enables a highly reconfigurable/programmable design. Furthermore, the pulse generator does not require an off-chip clock and the clock signals required for its operation are derived on-chip from the frequency synthesizer circuitry.

In order to detect targets over a wide range of 0.15 m to 40 m, a widely-tunable delay between the instants of pulse transmission and receiver correlation is necessary. Moreover, to achieve longer range and higher range resolution, it is desirable to incorporate variable prf and pulse width. These programmable parameters essentially provide a great deal of flexibility in designing radar DSP algorithms, leading to improved radar performance. For instance, longer pulse-widths (with pulse compression) can be transmitted to detect targets at longer ranges [1], [30]. Variable prf can be used to reduce ambiguities in either range (low prf) or Doppler velocity (high prf) [30]. To meet the aforementioned requirements, the CMOS baseband pulse generator, shown in Fig. 14, has been designed to generate pulses with widths ranging from 200 ps to 2 ns (pw[5:0]), with a variable prf of 1 MHz to 1.5 GHz (prf[12:0]). The delay between the TX and RX triggers can be tuned from 1 ns to 0.3 μs (delay[12:0]), corresponding to the 0.15-to-40-m radar range. An on-chip JTAG TAP interface is used to input the control bits of the pulse generator.

The constituent building blocks of the pulse generator are shown in Fig. 14. Timing diagrams of Fig. 15 illustrate the operation of the pulse generator. The prf generation circuitry consists of a 12-bit counter and is clocked by the 100-MHz reference of the dual-band frequency synthesizer. The 12-bit counter counts for a duration equal to 1/prf and generates a short pulse at the end of the count. The short pulse triggers the transmit enable (TX_EN) signal while the counter resets its count. The rising edge of TX_EN triggers a circuit which generates the transmit trigger (TX_Trig) sufficiently wide ($\approx$4 cycles of the trigger generator clock) for reliable operation of the monopulse generator. At the same time, another 12-bit counter (in the dual-trigger generator) is reset and its count duration is set equal to the desired delay between the transmit and receive triggers. As mentioned before, by varying this delay using *delay[12:0]*, targets in different range gates can be sequentially detected. At the end of the count, the receive enable signal, RX_EN, is set active and then generates the receiver trigger, RX_Trig. The 1.5-GHz clock required for the TX/RX trigger generation is derived from a divider output in the PLL loop.

The trigger signals, TX_Trig and RX_Trig, are each fed to separate monopulse generators (Fig. 14). The monopulse generator, whose schematic is shown in Fig. 14, derives the final baseband pulse from the trigger signal by a NOR operation of the original trigger signal and its delayed replica. The variable delay (and hence variable pulse width) is provided by a bank of binary weighted switched capacitors. By varying the capacitance using *pw[5:0]*, the capacitor charging time is varied resulting in variable delay between the nodes A and B in Fig. 14. Representative waveforms of the transmit pulse, TX_Pulse, and receive pulse, RX_Pulse, are shown in Fig. 15.

V. Measurement Results

A prototype of the dual-band TRX has been implemented in a 0.18-μm SiGe BiCMOS technology with six metal layers. The design utilizes the 0.15-μm HBTs with $f_T = 200$ GHz and $f_{\max} = 180$ GHz for processing MMW signals, while 0.18-μm MOSFETs are used for digital logic functions (including the high-speed pulse generator and the frequency synthesizer). Fig. 16 shows the die micrograph of the 3.9-mm $\times$ 1.9-mm dual-band TRX. The LNA is at the top left, the dual-band synthesizer at the top center, the pulse generator at the bottom

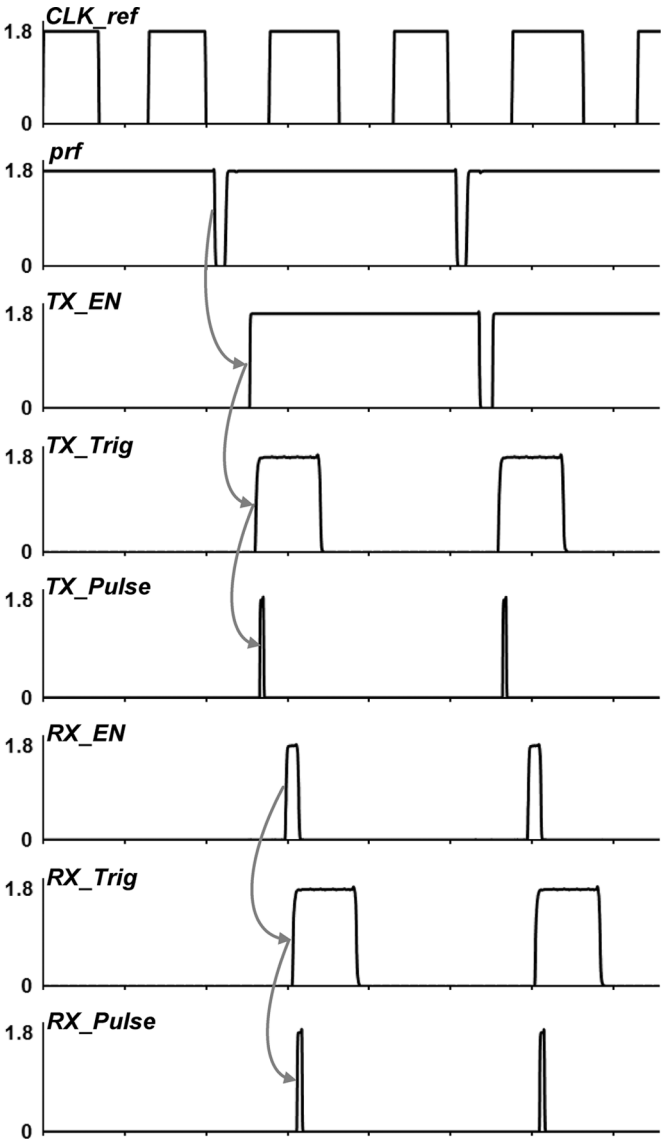

Fig. 15. Timing diagram of the pulse generator.

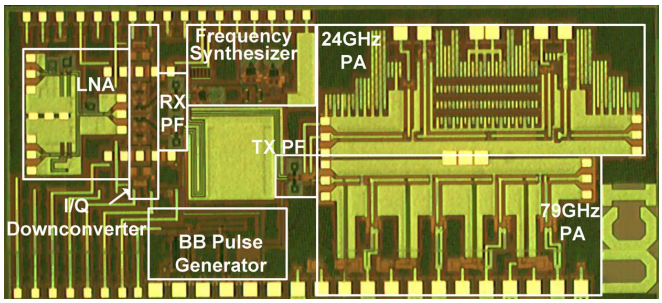

Fig. 16. Die micrograph of the 3.9 × 1.9-mm^2 dual-band transceiver chip.

center, and the power amplifiers occupy the right half of the chip.

As evident from circuit descriptions of Section IV and the die micrograph in Fig. 16, both transmission lines and spiral inductors have been used extensively in the MMW circuits in the TRX. The 2.8-μm-thick Al top metal, M_6, was used to realize inductors and transmission lines, while ground shields

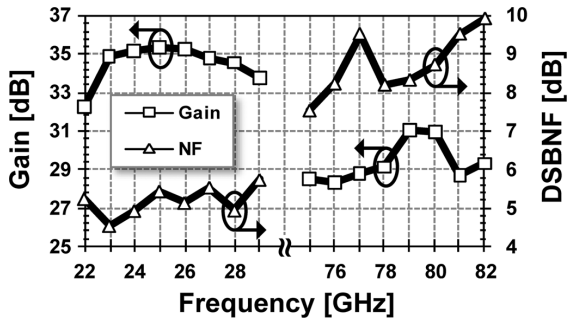

Fig. 17. Measured conversion gain and double-sideband noise figure of the dual-band receiver.

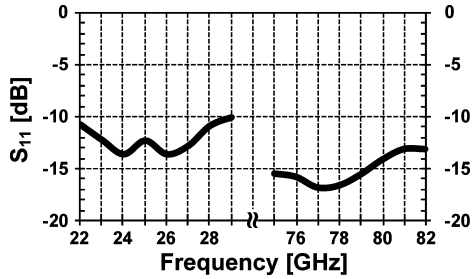

Fig. 18. Measured return loss at the receiver inputs in the two bands.

were laid out in bottom metal layer, M_1. Both microstrip and conductor-backed CPW structures were used for transmission lines in different parts of the design. The process also offers 2-fF/μm^2 MIM capacitors. Broadband lumped circuit models for passive devices were extracted from planar 3-D electromagnetic simulation results [38].

Similar to the synthesizer chip reported in [25], the dual-band transceiver chip has been characterized in a chip-on-board environment. All pads except the MMW signals were wirebonded to a PCB. These included dc supplies, digital signals of the JTAG, control voltages of the VCO and divider and the 50–125-MHz crystal reference signal for the frequency synthesizer. In addition to circuit breakouts on the prototype chip, flexibility of monitoring and debugging signals at the inputs and outputs of major circuit blocks was enabled by internal pads. These internal pads have been absorbed as part of the circuit design. All high-frequency input/output signals of the transceiver chip were wafer-probed. While a coaxial setup was sufficient for the 24-GHz mode, the 79-GHz mode required a hybrid setup consisting of both coaxial and WR-10 waveguide components. Since the measurement frequency of the available vector network analyzer (VNA) was limited to 67 GHz, a custom measurement setup based on a scalar network analyzer (SNA) was used to measure reflection coefficients.

On-wafer measurements of the receiver reveal power conversion gains of 32–35 dB and 28–31 dB in the 24-GHz and 79-GHz bands, respectively. As observed from the measured conversion gain in Fig. 17, the receiver 3-dB bandwidth encompasses the 22–29-GHz and 76–81-GHz automotive radar bands. Fig. 17 also shows the measured double-sideband noise figure (DSB-NF) of the receiver in the two bands. The receiver achieves a DSB-NF of 4.5–5.7 dB in the 22–29-GHz band and

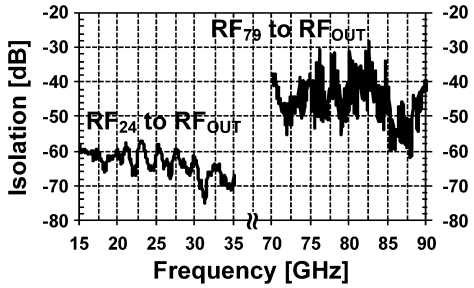

Fig. 19. Measured off-state isolation between LNA input and output in the two bands.

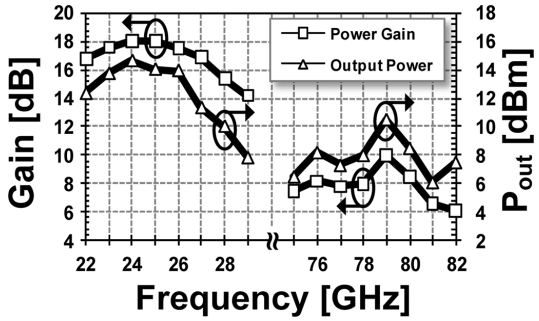

Fig. 20. Measured power gain and output P_{1dB} of the power amplifiers.

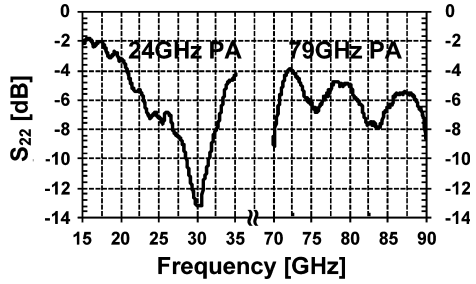

Fig. 21. Measured output return losses of the 24-GHz and 79-GHz power amplifiers.

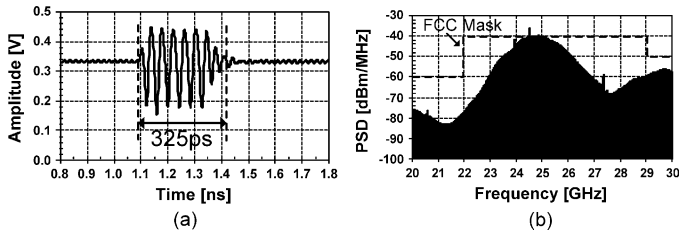

Fig. 22. Measured (a) time-domain waveform and (b) spectrum of the 24-GHz transmitter output pulse.

7.5–9.5 dB in the 76–81-GHz band. Fig. 18 shows the measured return losses at the two inputs of the receiver. The input match is better than −10 dB from 22-to-28 GHz and lower than −13 dB in the 76–81 GHz band. As described in detail in Section IV, when the LNA is in the off-state, the isolation between the LNA input and output should be high enough to prevent saturating the downconversion chain following the LNA. The measured off-state isolation is lower than −60 dB in the 24-GHz band and about −30 dB in the 79-GHz band, as depicted in Fig. 19. The receiver dissipates 107.5 mW and 162.5 mW in the 24-GHz and 79-GHz bands, respectively.

Fig. 20 depicts the power gain and output power at the 1-dB compression point of the MMW power amplifiers. The 24-GHz PA achieves a maximum power gain of 18 dB with a 3-dB bandwidth from 21 GHz to 28 GHz, and the 79-GHz PA achieves 10 dB gain with 75–80.5-GHz 3-dB bandwidth. The output P_{1dB} of the PAs are 14.5 dBm and 10.5 dBm in the 24-GHz and 79-GHz bands, respectively. The 24-GHz PA and the 79-GHz PA achieve power-added efficiencies (PAE) of 13.9% and 4.7%, respectively. The corresponding drain efficiencies are 14.2% and 5.4%. At the 1-dB compression point, the 24-GHz PA consumes 110 mA and the 79-GHz PA draws 115 mA, both from a 1.8-V supply. The measured output match of the PAs is better than −5 dB in the operating frequency bands, as shown in Fig. 21. The transmitter circuits dissipate 312.5 mW and 332.5 mW in the 24-GHz and 79-GHz bands, respectively.

The performance of the dual-band frequency synthesizer is characterized in the same fashion as described in [25]. The synthesizer achieves a locking range from 23.8 GHz to 26.95 GHz in the K band and from 78.4 GHz to 81.1 GHz in the W band. The loop bandwidth of the synthesizer is about 1 MHz. The closed-loop phase noises at the outputs of the 24-GHz and 79-GHz VCOs are −114 dBc/Hz and −100.4 dBc/Hz, respectively, at 1-MHz offset from the carrier. The reference spurs are at least 47 dB below the carrier in both bands. The synthesizer consumes 90 mW in the 24-GHz band and 120 mW in the 79-GHz band. The interested reader is referred to [25] for details of the software-based frequency-lock calibration and representative measurement results of the synthesizer.

The MMW pulse measurements were performed with the transmitter, baseband pulse generator, frequency synthesizer and pulse former enabled, and with the receiver turned off. The time-domain waveform of the pulse at the output of the 24-GHz PA, observed directly on a sampling oscilloscope, is shown in Fig. 22(a). The corresponding power spectral density in dBm/MHz is shown in Fig. 22(b) and meets the FCC mask except for an occasional spur. For this measurement, the LO frequency was set at the center of the band, i.e., 25.5 GHz, and the pulse-width was chosen to correspond to the maximum allowed bandwidth, i.e., 7 GHz. Fig. 23(a) and (b) show the time-domain waveform and the power spectral density, respectively, of the pulse at the 79-GHz PA output. Analogous to the 24-GHz measurement, the LO frequency and the pulse bandwidth in this case were set at 79 GHz and 4 GHz, respectively. The power spectral density is well below the allowed limit of 3 dBm/MHz. The LO leakage at 79 GHz can be clearly seen in Fig. 23(b). Note that the W-band signal was downconverted to a 4-GHz IF using a WR-10 waveguide mixer in order to enable measurement with lower-frequency spectrum analyzer. The x axis of the spectral plot in Fig. 23(b) has been scaled back to the W-band for clarity. Spectral nulls corresponding to pulse-widths of about 300 ps for the 24-GHz pulse and 1 ns for the 79-GHz pulse are readily observed in Figs. 22(b) and 23(b), respectively.

TABLE II
SUMMARY OF THE MEASURED PERFORMANCE

Receiver

	K Band	W Band
Conversion Gain	35 dB	31 dB
DSB Noise Figure	4.5 dB	8 dB
Input P1dB	−33.2 dBm	−30.7 dBm
I/Q Mismatch	<2°, <1.1 dB	<5°, <1.5 dB
Input Return Loss	< −10 dB	
Output Return Loss	< −15 dB	
LO-to-RF Leakage	< −70 dB	
LO-to-IF Leakage	< −38 dB	
Power Dissipation	107.5 mW	162.5 mW

Transmitter

Power Gain	18 dB	10 dB
Output P1dB	14.5 dBm	10.5 dBm
3dB Bandwidth	21-28 GHz	75-80.5 GHz
Power Dissipation	312.5 mW	332.5 mW

Frequency Synthesizer

Locking Range	23.8-26.95 GHz	78.4-81.1 GHz
Phase Noise @1MHz	−114 dBc/Hz	−100.4 dBc/Hz
Reference Spurs	<−49.5 dBc	<−47 dBc
Power Dissipation	90 mW	120 mW

Transceiver

Technology	0.18-μm BiCMOS (f_T/f_{max} = 200/180 GHz)	
Die Size	3.9 mm×1.9 mm	
Supply Voltage	2.5 V (Analog), 1.8 V (Digital)	
Power Dissipation	510 mW	615 mW

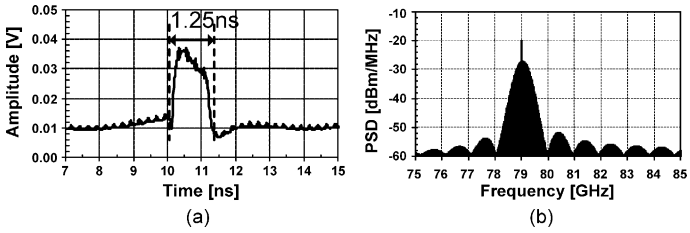

Fig. 23. Measured (a) time-domain waveform and (b) spectrum of the 79-GHz transmitter output pulse.

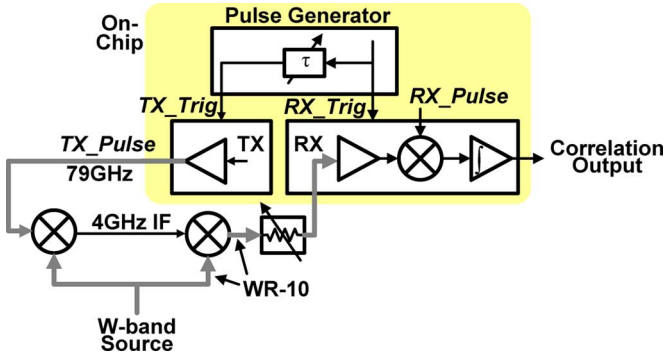

Fig. 24. Setup for the loopback measurement of the transceiver in the 79-GHz mode. WR-10 rigid waveguides are shown as thick grey lines.

The pulsed radar functionality of the transceiver chip can be verified either (i) through a wireless test or (ii) by inserting a tunable delay (on the order of the pulse repetition interval) between the transmitter output and the receiver input. Due to the unavailability of antennas and widely tunable delay lines at the operating frequencies of the transceiver, an alternative method of radar functionality verification has been devised. This method consists of emulating the delay between the transmitted and received pulses on-chip through the baseband pulse generator. Off-chip components are still required to provide an attenuated version of the transmitter output at the receiver input. The overall radar loopback setup, when the transceiver operates in the 79-GHz mode, is depicted in Fig. 24. Due to the mechanical rigidity of the WR-10 waveguides used for W-band signals, the attenuated output of the transmitter cannot be directly connected to the receiver input. Therefore, the 79-GHz transmitter output is first downconverted to a 4-GHz IF using a waveguide mixer. The signal is then supplied to a waveguide upconversion mixer through a coaxial cable. The resulting W-band output is attenuated and fed to the receiver input. When the transceiver is operating in the 24-GHz mode, a fully-coaxial setup is possible and no frequency conversion is required. As shown in Fig. 24, the delay τ between the transmit trigger, TX_Trig, and the receive trigger, RX_Trig, is generated by the baseband pulse generator. This delay, in effect, introduces an offset between the transmitted pulse, TX_Pulse, and the received pulse, RX_Pulse. By varying τ, the correlation function of the receiver can be generated. As explained before, due to the power-limited transmit mask in the 24-GHz band and the high path loss in the 79-GHz band, several pulses need to be integrated to increase the signal above the noise floor. The radar correlation function after coherent integration of 500 pulses is shown in the plot of Fig. 25 for a 1-ns-wide pulse, corresponding to a range resolution of

TABLE III
COMPARISON OF STATE-OF-THE-ART 24-GHz TRANSCEIVERS

	Frequency (GHz)	Technology f_T/f_{max} (GHz)	RX Gain (dB)	RX NF (dB)	Phase Noise[a] (dBc/Hz)	TX Pout (dBm)	DC Power (W)	Chip Area (mm^2)
[4]	22-26	0.13-µm SiGe BiCMOS	30	6	−104	3	0.37	9
[5]	22-26	0.13-µm SiGe BiCMOS 170 GHz	47	3	−104.3	1.5	0.64	5.9
[14]	24	0.13-µm CMOS	31	15 (Array)	−105	12.9	TX: 0.98 RX: 0.52	5.1
[2]	22-26	SiGe HBT 80 GHz	45	7.8	-	-	1.08	-
[15]	22-24	0.13-µm CMOS	12	7.5	-	-	0.11	3.02
[16]	24	0.18-µm SiGe BiCMOS 120 GHz	43	7.4	−103@19.2 GHz	-	0.91	11.55
[29]	22-29	0.18-µm CMOS 55 GHz	38	5.5	−107	-	0.13	3
[39]	24	0.13-µm CMOS	3.2	10 (LNA)	-	-	0.04	0.58
[40]	24	0.18-µm CMOS 60 GHz	28.4	6	−110@19.1 GHz	-	0.05	1.32
[41]	24	0.18-µm CMOS	27.5	7.7	-	-	0.06	0.2
[42]	23-25	65-nm CMOS	31.5	6.5	−110	-	0.09	2.1
[17]	24	0.18-µm CMOS	-	-	-	14	1.97	14.28
[43]	24	0.13-µm CMOS	-	-	−95.7@19.9 GHz	7	TX: 0.12 PLL: 0.04	TX: 2.2 PLL: 0.8
This Work	**22-29**	**0.18-µm SiGe BiCMOS 200/180 GHz**	**35**	**4.5**	**−114**	**14.5**	**0.51**	**7.4**

[a]Phase noise at 1-MHz offset from a carrier frequency within the operating frequency range, unless otherwise noted.

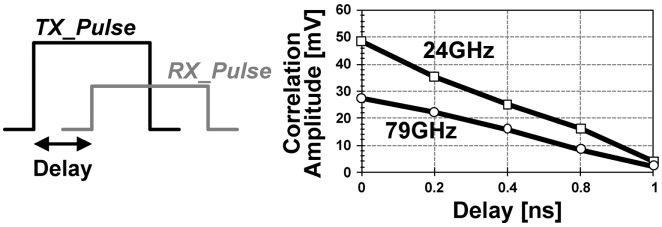

Fig. 25. Measured correlation output as a function of the delay between the transmitted and received pulses.

15 cm. As the delay is increased, the correlation output decreases due to the decreasing overlap between the two pulses. The delay in Fig. 25 is varied in steps of 200 ps corresponding to a range accuracy of 3 cm. The signal level at the receiver input (i.e., the attenuator output) is set to −80 dBm for this measurement. This power level is restricted by the lower limit of the equipment and does not represent the minimum detectable signal of the receiver.

A 2.5-V supply is used for the analog circuits, with the exception of the PAs which run off a 1.8-V supply. Another 1.8-V supply drives the digital CMOS circuits. The entire transceiver dissipates 510 mW in the 24-GHz mode and 615 mW in the 79-GHz mode. In contrast, a 79-GHz transmitter reported in [8] for short-range radar applications dissipates 4.1 W. Table II summarizes the measured performance of the transceiver. Tables III and IV provide comparisons of the dual-band transceiver with single-band prior art in the 24-GHz and 77/79-GHz bands, respectively.

VI. CONCLUSIONS AND FUTURE WORK

In this paper, a new dual-band architecture for MMW transceivers, operating in the 22–29-GHz and 76–81-GHz automotive radar bands, has been presented. A highly-integrated TRX prototype chip has been designed and implemented in a 0.18-μm BiCMOS technology. Measurements of the fabricated prototype demonstrate excellent results. In the receive mode, a conversion gain of 35/31 dB and DSBNF of 4.5/8 dB have been obtained in the 24/79-GHz bands. Output powers of 14.5 dBm in the K band and 10.5 dBm in the W band have been achieved in the transmit mode. Radar functionality has been verified using loopback measurements. Detailed design and analysis of the key building blocks of the transceiver have been described. To the authors' best knowledge, this work is the first reported integration of high-speed digital circuitry with an MMW automotive radar transceiver in the W-band.

The architecture presented in this work enables low-cost low-power compact integration of 24-GHz and 77/79-GHz radar transceivers. Further investigation and research are needed for more efficient dual-band quadrature signal generation. Development of novel architectures for integration of dual-band phased

TABLE IV
COMPARISON OF STATE-OF-THE-ART 77/79-GHz TRANSCEIVERS

	Frequency (GHz)	Technology f_T/f_{max} (GHz)	RX Gain (dB)	RX NF (dB)	Phase Noise[a] (dBc/Hz)	TX Pout (dBm)	DC Power (W)	Chip Area (mm^2)
[6]	76-81	0.13-µm SiGe HBT 170/200 GHz	25.6	9	−99	5.8	0.74	1.17
[6]	77-85	0.13-µm SiGe HBT 200/300 GHz	40	3.85	−99	11.5	0.78	1.17
[7]	76-77	0.18-µm SiGe HBT 200/275 GHz	14.2	17.7	−75.3@100 kHz	8	3.3	6.82
[18], [19]	76-80	0.12-µm SiGe BiCMOS 200/250 GHz	37	8	−95@54 GHz	12.5	2.77	25.8
[20]	77	90-nm CMOS	3.5	6.8 (LNA)	−86	6.3	0.92	2.88
[9]	76.5	0.18-µm SiGe HBT 195/290 GHz	30	7 (LNA)	-	12.5	-	TX: 3.8 RX: 4.3
[10]	75-82	0.18-µm SiGe HBT 200/275 GHz	32	11 (SSB)	-	-	1.1	1.1
[11]	75-78	0.14-µm SiGe HBT 225/330 GHz	30	11.5 (SSB)	-	-	0.44	1.16
[12]	68-76	0.19-µm SiGe BiCMOS 220/250 GHz	24	4.8	−98	-	0.12	0.23
[44]	73-77	0.13µm SiGe BiCMOS 200/250GHz	46	7	−93@70.5 GHz	-	0.19	1.7
[13]	79	0.25-µm SiGe BiCMOS 180/200 GHz	26	-	−90	-	0.59	1.26
[8]	79	0.14-µm SiGe HBT 200/300 GHz	-	-	−96	1.5	4.12	1.16
This Work	**76-81**	**0.18-µm SiGe BiCMOS 200/180 GHz**	**31**	**8**	**−100.4**	**10.5**	**0.61**	**7.4**

[a]Phase noise at 1-MHz offset from a carrier frequency within the operating frequency range, unless otherwise noted.

arrays is also a topic of future research. Multiple-mode phased arrays in the 77/79-GHz bands will ultimately enable integrated short-range and long-range detection using a single chip.

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