# The World's First Fully Integrated 210GHz Fundamental Frequency Transceiver in CMOS

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Abstract — This paper presents the world's first fundamental frequency CMOS 210GHz transceiver. The transmitter (TX) employs a 2×2 spatial combining array consisting of a doublestacked cross-coupled VCO at 210GHz with an on-off-keying (OOK) modulator, a power amplifier (PA) driver, a novel balunbased differential power distribution network, four PAs and an on-chip 2x2 dipole antenna array. The non-coherent receiver (RX) utilizes a direct detection architecture consisting of an onchip antenna, an LNA, and a power detector. The TRX chip is fabricated in a 32nm SOI CMOS process (f<sub>T</sub>/f<sub>max</sub>=250/320GHz). The VCO generates measured -13.5dBm output power; and the PA shows a measured 15dB gain and 4.6dBm P<sub>sat</sub>. The LNA exhibits a measured in-band gain of 18dB and minimum inband noise figure (NF) of 11dB. The TX achieves an EIRP of 5.13dBm at 10dB back-off from saturated power. It achieves an estimated EIRP of 15.2dBm when the PAs are fully driven. This is the first demonstration of a fundamental frequency CMOS TRX at the 200GHz range.

## I. INTRODUCTION

The vastly under-utilized spectrum in the millimeterwave/THz frequency range enables disruptive applications including 10-gigabit chip-to-chip wireless communications and imaging/spectroscopy. On the imaging applications front, THz imaging is considered to be one of the emerging technologies [1]. the availability of broad unlicensed frequency spectrum across the millimeter-wave/THz frequency range unfolds new ideas on super-precise sensing at micrometer-level and multi-10-gigabit instant wireless access at the centimeter-level spacing between transmitter (TX) and receiver (RX) [4]-[5]. Today, THz front-ends are mainly implemented using Schottky diodes [6], nonlinear optical [7], [8], or III-V devices [9]. A complete transceiver (TRX) in a 50 nm mHEMT technology has been developed for wireless links with up to 25Gbit/s data rate at 220GHz [10]. Owing to aggressive scaling in feature size and device  $f_T/f_{max}$  (Fig. 1), nanoscale CMOS technology potentially enables integration of sophisticated systems at THz frequency range, once only be implemented in compound semiconductor technologies. Recently, CMOS THz signal sources and TRXs have been reported [11]-[14], employing techniques such as distributed active radiator (DAR) and super-harmonic signal generator.



Fig. 1. ITRS 2008

This paper demonstrates the first 210GHz TRX with OOK modulation in a 32nm SOI CMOS process

(fT/fmax=250/320GHz). This fundamental frequency TRX incorporates a  $2\times2$  TX antenna array, a  $2\times2$  spatial combining power amplifier (PA), a fundamental frequency voltage-controlled oscillator (VCO), and an LNA. Short range wireless test was carried out, showing the possibility of wireless 20Gbit/s data rate for chip-chip communications.

## **II. SYSTEM ARCHITECTURE**

Harmonic-based TRXs reported to date in (Bi-)CMOS processes [13], [14] all suffer from high power consumption and noise figure (NF) due to the lack of front-end amplification. On the TX side, the frequency multiplier - placed usually as the last stage prior to antenna – exhibits negative power gain (e.g., -10dB). Therefore, to generate adequate output power, a stronger signal (e.g., 10dB higher) than the TX power needs to be generated by a lower frequency pre-PA, thus resulting in low efficiency and high power consumption. On the RX side, due to lack of LNA in the chain, the noise contribution from the subsequent stages cannot be suppressed, thereby leading to poor NF and poor RX sensitivity.

This work addresses the above issues by implementing a TRX architecture that operates at TRX's fundamental frequency. The TRX system architecture is shown in Fig. 2 [15], and is integrated in a nanoscale CMOS process alongside on-chip antenna array. It employs fully differential topology, as it is inherently robust to common-mode substrate and power/ground induced noise and exhibits better linearity than single ended topology.



The TX incorporates a  $2\times2$  spatial power combining array architecture, consisting of a new double-stacked crosscoupled VCO at 210GHz with an OOK modulator, a PA driver, a novel balun-based differential power distribution network, four PAs and on-chip  $2\times2$  dipole antenna array. The non-coherent RX employs a direct detection architecture comprising an on-chip antenna, an LNA, and a power detector. The balun-based differential power distribution network, which is amenable to high frequencies. these unwanted cross-overs are avoided by using a pattern of alternate power splitter and balun instead of using two stage power splitters.

#### III. ON-CHIP ANTENNA ARRAY AND BALUN DESIGN

Fig. 4(a) shows an on-chip dipole antenna with surrounding ground shield, which is integrated in a 32nm SOI CMOS process with a substrate resistivity of  $13.5\Omega$ -cm. The high conductivity of the low resistivity substrate of a CMOS process compared to off-chip substrate is one of the most crucial contributors to the poor radiation efficiency of on-chip antenna. The substrate thickness of 300µm (i.e., the default post fabrication thickness) at 210GHz is close to  $\frac{3}{4}\lambda$  in the substrate, the constructive reflection from the ground underneath the silicon substrate will help boost the radiation efficiency to as high as 24%, as shown in Fig. 4(b).



A 2×2 antenna array with 0.57 $\lambda$  spacing between elements (i.e., 820 m) at 210GHz is designed to achieve a high directivity [16]. For frequencies from 200- to 220-GHz, the simulated antenna coupling in the E- and H-planes stays less than 220dB and 30dB, respectively. This low mutual coupling guarantees a negligible effect on the array's attributes, such as array factor and input impedance.

Fig. 7 shows the balun structure, incorporating a cascade of two quarter-wavelength couplers. To achieve  $50\Omega$  input matching (S11 = 0), the odd and even impedances, Zoo and Zoe, of the quarter-wavelength coupler in the balun should be 26- and 96- $\Omega$ , respectively [17]. Although both Zoo and Zoe are varied with the interlayer dielectric thickness, the width of signal line, and the spacing between signal and ground lines, strict constraints exist on these geometrical parameters in a CMOS process. This makes it difficult to design the coupler to achieve the desired Zoo and Zoe values. A vertical coupler structure with overlapping offset is thus employed to realize the Marchand balun. This offset is introduced to provide additional degree of freedom in adjusting Zoo and Zoe. The balun's bandwidth is greater than 100GHz. Amplitude imbalance between Ports 2 and 3 is only 0.2 dB, while phase imbalance is less than  $\pm 2\Box$  around 180° over the 100GHz bandwidth.



## III. 210 GHZ POWER AMPLIFIER, LNA, AND VCO

Fig. 15 shows the schematic of the 210GHz CMOS PA, which is comprised of a three-stage differential amplifier using *over-neutralization* technique. Differential topology eliminates the parasitics' source degenerative effects by

providing shorter physical interconnection from its transistors' source terminals to ground compared to a singleended counterpart, and is also insensitive to the modeling inaccuracy of decoupling capacitors at 210GHz. In addition,  $C_{gd}$ -neutralization capacitor is simply realized by  $C_{gd}$  of a similar MOSFET to mitigate the mismatch between neutralization capacitor and main transistor's  $C_{gd}$ , as shown in Fig. 16(a).

The transistor's intrinsic  $G_{max}$  after layout is only 4.5dB and after deducting the loss of matching network (roughly 2.5dB per stage), the achievable power gain per stage is only 2dB. In order to overcome this problem, over-neutralization technique has been employed. The PA's main transistors are intentionally pushed to the edge of stability region, resulting in higher gain shown in Fig. 16(b). By choosing proper neutralization capacitance C<sub>n</sub>, the  $G_{max}$  can be boosted by as much as 4dB. To leave a margin for stability, a 3dB gain boost, corresponding to  $K_f$  of 1.1, is chosen.

All PA stages are interstage-matched to  $50\Box$  to make the design more robust to process-dependent uncertainties in passive components at this frequency, which, in turn, leads to more flexibility in layout. The PA's output matching network is designed for maximum Psat. The extra loss added by matching network makes the amplifier more stable, the stability factor of the overall PA is greater than unity at all frequencies, which means it is unconditionally stable.

The PA core occupies  $150 \times 400 \mu m^2$  of die area (excluding pad). The PA breakout was tested by using a Gband (140-220GHz) RF probe and power meters. To this end, on-chip baluns were used to convert the input and output differential signals to single-ended. The loss of the on-chip balun was calibrated using back-to-back configuration and was de-embedded from the PA output power. The PA circuit exhibits a measured peak gain of 15dB, OP1dB of 2.7dBm, Psat of 4.6dBm, and a peak PAE of 6%, as shown in Fig. 17(a). Fig. 17(b) exhibits a 3-dB bandwidth of more than 14 GHz. The measured PA bandwidth is limited by the highest measurable frequency (220GHz) of the test equipment.



Fig. 15 210GHz CMOS power amplifier schematic



As was discussed in the previous section, the transconductance gm degrades significantly as the operation frequency increases towards half- $f_{max}$  of the device. Moreover, varactor loss becomes the dominant contributor to the Q factor degradation of the oscillator. As a consequence,

new circuit techniques need to be examined in the design of a fundamental VCO at 200GHz to overcome these limitations. Inductive tuning was demonstrated to be amenable to high frequencies compared to varactor tuning [31].

One effective way of realizing the negative resistance is by another cross coupled pair. However, the corresponding parasitic capacitance cannot be neglected. Fig. 20(b) shows its effective parallel resistance Rp and parallel capacitance Cp at 200GHz for circuit with source degeneration of both negative resistance Rs and parasitic capacitance Cs in Fig. 19(b). It indicates that both Rp and Xp (=1/(j $\omega$ Cp)) are lowered as the source parasitic capacitance Cs increases. Therefore, an extra inductor Ls is added between the source terminals of the cross coupled pair to resonate out this undesired parasitic capacitance (Fig. 19(b)).

Fig. 21 shows the fundamental double-stacked crosscoupled VCO and the OOK modulator. The overall negative resistance of this oscillator is increased due to an additional negative source degeneration resistance provided by M1-M2. This negative resistance compensates for the excessive varactor loss at very high frequencies, thereby improving overall loop gain. As mentioned above, the 30pH inductor LS in Fig. 21 mitigates the detrimental effect of parasitic capacitance of the bottom cross-coupled pair M1-M2. The interstage matching network between the VCO buffer and the OOK modulator has been realized by transformers, thereby leading to compact layout. The OOK modulator utilizes a cascode topology M7(M8)-M9(M10), where the modulated signal is applied to the gate of transistor M9(M10). The output of the OOK modulator is matched 50 $\Omega$  using transformers.



The VCO core and modulator occupies 100×400µm2 of die area. The circuit was characterized using a G-band (140GHz-220GHz) RF probe, power meters and sub-harmonic mixer. The VCO exhibits a measured output power of -13.5dBm, a tuning range of 8GHz (204.7-212.7GHz), and a phase noise of -81dBc/Hz at 1MHz offset at 209GHz (Fig. 22). The VCO plus the buffer and OOK modulator consumes a total of 42mA from 1V supply.



Fig. 4 shows the schematic of the 7-stage differential CGD-neutralized LNA. At 210GHz, only one gain stage is incapable of providing enough gain to mitigate the noise contribution of subsequent stages. Therefore, the second stage needs to be optimized for noise, as well. The LNA design methodology of each stage has progressively moved from minimizing noise figure to maximizing gain. Inductive degeneration is employed in the first two stages such that Zs,opt=Zin\*, where Zs,opt denotes the optimum source impedance. Simultaneous power and noise match is thus achieved. In addition, inductive degeneration reduces the NFmin [6]. 4th-order matching networks have been used for wideband interstage and output matchings in the last 5 stages. However, lower-order matching networks are used for the first stages, since the loss of passive components at these stages severely degrades the NF. The LNA achieves a measured peak gain of 18dB with a BW of, at least, 14GHz. Input/output return losses are better than -8dB. The LNA draws 44.5mA from 1V supply, and occupies 0.65×0.4 mm2 of chip area.



In addition, the received signal cannot always be amplified to the ADC's full scale in a rectangular quantizer, since the RF gain steps are discrete. As a result, the full resolution of ADCs is not always utilized. To guarantee an acceptable quantization noise, the ADC resolution should thus be chosen high enough to account for this under-utilized full scale. On the contrary, the maximum phase variation in the phase path is independent of the signal level, varying between  $0^{\circ}$  to  $360^{\circ}$ . Therefore, the phase quantization path does not suffer from resolution reduction, caused by discrete nature of gain steps.

#### **IV. MEASUREMENTS**

The TRX chip is fabricated in a 32nm SOI CMOS process with a substrate resistivity of  $13.5\Omega$ -cm. The array elements are separated by 820µm, which corresponds to approximately  $0.57\Box\lambda$  at 210GHz. The TX chip's radiated power is captured by a 21dBi VDI WR-5.1 horn antenna, and is then detected by a WR-5.1 detector. Accounting for 61.8dB path loss - estimated by Friis formula - for a distance of 14cm at 210GHz, the captured power translates to a broadside EIRP of 5.13dBm. The measured beamwidth of transmitter is 57 $\square$  and 54 $\square$  at 208GHz and 212GHz, respectively. A modulated continuous wave (CW) wireless testing between TX and RX chip was performed over 3.5cm distance, and the measured SNR for different CW frequencies is shown in Fig. 5. Considering that the TRX system operates in linear region (TX is 8dB back off from OP1dB), the thermal noise limits the performance of the wireless links rather than non-linearity. In this case, with the requirement of SNR of 13dB (corresponding to BER of 10-5 for non-coherent OOK modulation), the maximum data rate is 20Gbps. The RX sensitivity of -47dBm corresponds to an RX NF of around 12dB.

The complete measured performance of the TRX is summarized in Fig. 6. The TX and RX consume 240mW and 68mW, respectively. The TX achieves EIRP of 5.13dBm with 3dB bandwidth of more than 14GHz. The VCO shows - 13.5dBm output power; the PA shows a measured 15dB gain and 4.6dBm  $P_{sat}$ . The LNA shows a measured gain of 18dB. The die photos of the TX and RX occupying areas of 1.4×2.5mm2 and 0.8×1.4mm2, respectively (including pad ring) are shown in Fig. 7.







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	[11]	[12]	[13]	[14]	This work
Technology	45nm SOI CMOS	45nm SOI CMOS	0.13µm BiCMOS	65nm CMOS	32nm SOI CMOS
Frequency	291GHz	280GHz	380GHz	260GHz	210GHz
Architecture	2×2 DAR	4×4 DAR	Quadrupler-based TRX	2×2 Quadrupler- based TRX	2×2 Fundamental TRX
Modulation	None	None	FMCW	OOK	OOK
EIRP [dBm]	-1	9	-13	5	5.13 (15.2 @ P <sub>sat</sub> ) *
P <sub>DCTX</sub> [mW]	74.8	430	182	688	240
EIRP/P <sub>DCTX</sub>	1.1%	2%	0.028%	0.46%	1.4% (>6.9% @ P <sub>sat</sub> ) *
Area [mm <sup>2</sup> ]	0.64	7.29	4.18	6	3.5(TX) + 1.12(RX)

\* The EIRP if the PAs are fully driven is 15.2 dBm (4.6dBm  $P_{sat}$  of one PA + 6dB combining gain + 4.5dBi antenna gain). With a stronger PA driver, the power consumption is assumed to get doubled (a conservative estimation) to be 480mW, and the expected EIRP/P<sub>DCTX</sub> is 6.9%.

#### Table 1 Comparison table