W-Band Silicon-Based Frequency Synthesizers Using Injection-Locked and Harmonic Triplers

Chun-Cheng Wang, *Student Member, IEEE*, Zhiming Chen, *Student Member, IEEE*, and Payam Heydari, *Senior Member, IEEE*

***Abstract*—Two monolithically integrated W-band frequency synthesizers are presented. Implemented in a 0.18 μm SiGe BiCMOS with $f_T/f_{\max}$ of 200/180 GHz, both circuits incorporate the same 30.3–33.8 GHz PLL core. One synthesizer uses an injection-locked frequency tripler (ILFT) with locking range of 92.8–98.1 GHz and the other employs a harmonic-based frequency tripler (HBFT) with 3-dB bandwidth of 10.5 GHz from 90.9–101.4 GHz, respectively. The measured RMS phase noise for ILFT- and HBFT-based synthesizers are 5.4° and 5.5° (100 kHz to 100 MHz integration), while phase noise at 1 MHz offset is -93 and -92 dBc/Hz, respectively, at 96 GHz from a reference frequency of 125 MHz. The measured reference spurs are < -52 dBc for both prototypes. The combined power consumption from 1.8- and 2.5-V is 140 mW for both chips. The frequency synthesizer is suitable for integration in millimeter-wave (mm-wave) phased array and multi-pixel systems such as W-band radar/imaging and 120 GHz wireless communication.**

***Index Terms*—Colpitts, frequency generation, frequency multipliers, frequency synthesis, frequency synthesizer, injection-locked oscillators, millimeter-wave oscillators, multi-channel, phase locked loops, triplers, VCOs.**

I. Introduction

A CRITICAL building block in a W-band (75–110 GHz) imaging system [1], [2], a point-to-point communication (i.e., 81–86 and 92–95 GHz bands) [3], a 100-Gbps Ethernet, and a 120 GHz wireless transceiver [4] is a high performance low noise PLL. A number of W-band frequency synthesis techniques have recently been realized in SiGe BiCMOS [5]–[7] and CMOS [8]–[11] technologies. In [5], a fundamental 90 GHz PLL with closed-loop phase noise of -98.2 dBc/Hz @ 1 MHz offset was presented. However, the synthesizer has used a 5.6 GHz reference clock. In [8], using a 375 MHz reference frequency, a 96 GHz PLL phase noise of -75.6 dBc/Hz @ 1 MHz offset was measured. Using an offset mixer for generation of W-band signal, [9] achieves a measured phase noise of -63 dBc/Hz @ 0.25 MHz offset at 83.3 GHz output.

As the operation frequency (f_0) increases, the implementation of low phase-noise fundamental PLL will become increasingly challenging. In an integrated PLL-based frequency synthesizer, assuming VCO phase noise dominates and other blocks in the PLL contribute negligible noise, the RMS phase noise is roughly given by [12]

$$\sigma_{\phi}^{\mathrm{PLL}} = \Delta f \sqrt{\frac{\pi \cdot S_{\mathrm{VCO}}}{f_L}} \tag{1}$$

where S_{VCO} is the single-sideband phase noise of the free-running VCO at the offset Δf from the carrier, and f_L is the loop bandwidth. The term S_{VCO} is given by Leeson's equation and is proportional to $[f_o/(2\,V_o Q \Delta f)]^2$, where V_0 and Q are the oscillation amplitude and the tank quality factor, respectively.

Several factors contribute to difficulty of achieving low phase-noise PLL at mm-wave frequencies. From Leeson, the VCO's phase noise is expected to degrade in proportion with f^2. Moreover, the tank Q begins to be dominated by capacitances, and in particular, varactors as their Q degrades with increasing frequency (simulated Q of <3 at 96 GHz). Large $\mathrm{K_{VCO}}$ values on the order of GHz/V are commonly attained in W-band VCOs [5], [8]. Design techniques such as segmentation with switched capacitor or varactor, which is commonly used in VCO design to reduce $\mathrm{K_{VCO}}$ are not effective for VCO whose resonant frequency is closer to $f_{\max}$. This is because device and interconnect parasitic starts to dominate the overall capacitance, leaving little room for any form of segmentation capacitors.

Additionally, for a VCO with a large $\mathrm{K_{VCO}}$ inside a PLL loop, this results in a large up-conversion of noise coming from charge pump and loop filter to PLL's center frequency. Finally, a fundamental-frequency VCO must be accompanied by a fundamental divider, which consumes considerable power if a static architecture is used; or may limit the PLL locking range if an injection-locked [8] divider is used.

In comparison, a synthesizer comprising a subharmonic PLL followed by a frequency multiplier ($\times$ M) [13] allows a larger tuning range and a lower phase noise. Though the in-band phase noise in this synthesizer is magnified by $20\log_{10}$(M) due to frequency multiplication, this degradation would be exactly offset by the f_0^2 term in Leeson's equation, leaving the improvement in Q, output swing (V_0) and tuning range as added bonuses to overall phase noise improvement. Furthermore, practical mm-wave systems will require relatively large phased arrays [14] or multi-pixels [1]. This solution readily lowers the PLL's operation frequency, thereby making LO routing and distribution suitable for these systems.

In this paper, we present two single-chip 96 GHz frequency synthesizers using a fully-integrated 32 GHz PLL followed by frequency tripler. Two different types of triplers are designed. The first type leverages the idea of injection-locking oscillators

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The authors are with Nanoscale Communication IC (NCIC) Laboratory, University of California, Irvine, CA 92697 USA (email: ccw@uci.edu; zhimingc@uci.edu; payam@uci.edu).

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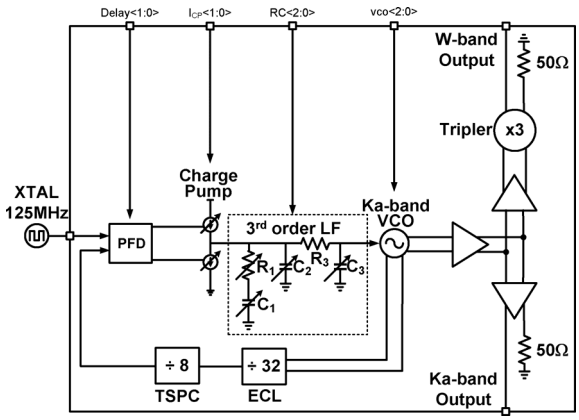


Fig. 1. Block diagram of the W-band frequency synthesis.

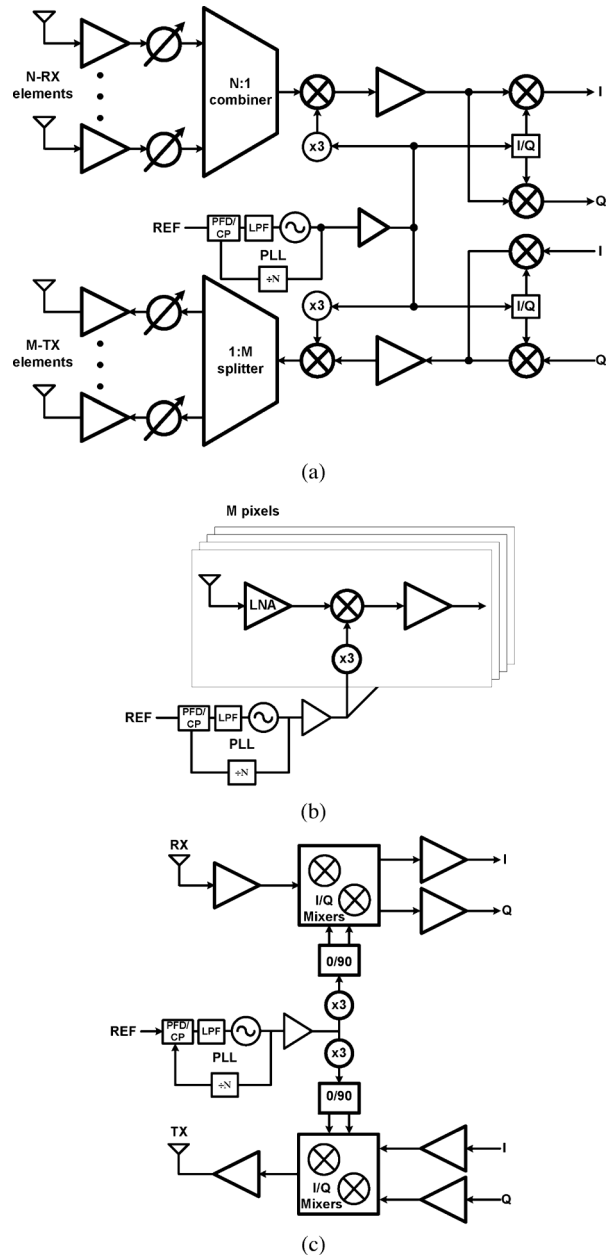
(ILOs) and injects a signal into the oscillator at subharmonic frequency using a harmonic generator [15], referred hereafter, as injection-locked frequency tripler (ILFT). The second type is based on harmonic generation and amplification, which generates the harmonics of the input signal, amplifies the desired harmonic, and filters out all other harmonics [13], referred hereafter as, harmonic-based frequency tripler (HBFT). The design has been implemented in a 0.18 μm SiGe BiCMOS process featuring bipolar transistor with $f_T/f_{\max} = 200/180$ GHz. The PLL system is targeted for integration within a 96 GHz multi-pixel passive imaging system [1]. It can potentially be used in emerging 120 GHz dual-conversion phased-array systems, as described later.

The paper is organized as follows. Section II discusses the architectural considerations for the PLL. The circuit design and analysis of key building blocks of the PLL are described in Section III. In Section IV, the harmonic generation using SiGe HBT is described. Section V focuses on the design of ILFT and HBFT. In Section VI, experimental results of the PLL system are presented and discussed. A comparison between the two chips is discussed in Section VII. Finally, Section VIII provides concluding remarks.

II. Frequency Synthesis

The system architecture of the W-band frequency synthesizer is depicted in Fig. 1. Low-order multipliers (i.e., doublers or triplers) are more amenable to on-chip active implementation since they rely upon the nonlinearity of the transistor, where the harmonic energy decreases with frequency. In this work, the W-band signal is synthesized by cascading a frequency tripler after a Ka-band (30.3–33.8 GHz) PLL. Chip A incorporates the ILFT, whereas Chip B uses the HBFT after the PLL.

The Ka-band PLL is comprised of a differential Colpitts VCO, a frequency divider chain with the division ratio of 256, a phase/frequency detector (PFD), a charge pump (CP), and a 3rd-order loop filter (LF). The divider chain utilizes ECL and CMOS CML circuits to realize asynchronous divide-by-32 and synchronous TSPC circuits to implement divide-by-8. Programmable PFD delay, CP current, and loop BW compensate for model inaccuracy and PVT variation. To facilitate *in situ* characterization of the PLL, an additional GSG pad was used to monitor the PLL's output.



(a)

(b)

(c)

Fig. 2. Possible frequency synthesis with this PLL: (a) 120 GHz heterodyne architecture, (b) 96 GHz direct-conversion passive imaging, and (c) 96 GHz direct-conversion active imaging/communication.

Fig. 2 illustrates three possible LO generation and distribution schemes that can be implemented using the PLL system depicted in Fig. 1. Fig. 2(a) proposes a dual-conversion zero-IF superheterodyne 120 GHz phased-array transceiver. The 30 GHz LO signal is routed to both the RX and TX, where it drives a tripler and an I/Q generator to perform frequency conversion. Fig. 2(b) shows an M-pixel 96 GHz direct-conversion passive imaging receiver. In this case, since phase carries no information, there is no need for I/Q, and the LO is distributed to M-pixel local triplers for zero-IF downconversion. A direct-conversion 96 GHz TRX for active imaging/communication is depicted in Fig. 2(c). Here, the LO is distributed to both RX and TX for both down- and up-conversion.

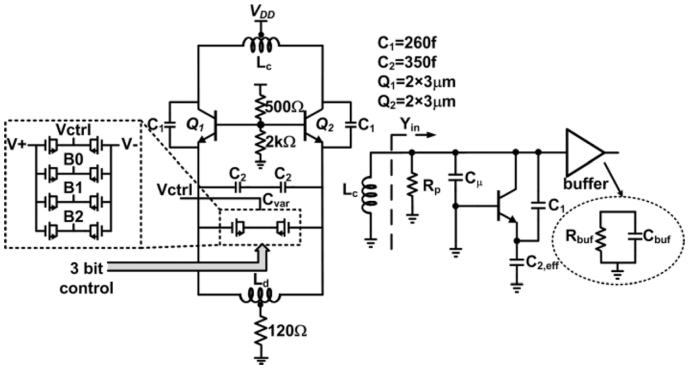


Fig. 3. Schematic and equivalent circuit model for 32 GHz Colpitts VCO.

From the above discussion, the W-band frequency synthesis presented in this work is amenable to multi-channel systems and can meet stringent phase noise requirements. Hence, this PLL system can potentially serve as the LO generation and distribution of several W-band applications as well as 120 GHz high data-rate communication. Next, the circuit design details of key building blocks of the PLL are described.

III. PLL Building Blocks

A. Colpitts Ka-Band VCO

A differential common-base Colpitts VCO with inductive degeneration is chosen for better phase noise performance [16]. The circuit schematic of the 32 GHz VCO is shown in Fig. 3. Symmetrically center-tapped inductors are used for both the load ($L_C = 150$ pH and $Q = 15$) and emitter degeneration ($L_d = 600$ pH and $Q = 12$). The resonance frequency of the degeneration tank, $\omega_{\rm DEG} = 1/\sqrt{L_E(C_2 + C_{\rm var})}$, ($L_E = L_d/2$) occurs below the oscillator's resonance frequency ($\omega_{\rm osc}$), such that the degeneration impedance becomes capacitive [17] with an effective capacitance $C_{2,\rm eff}$ expressed as $C_{2,\rm eff} = (C_2 + C_{\rm var})[1 - (\omega_{\rm DEG}/\omega)^2]$, at $\omega = \omega_{\rm osc}$. Tail current sources composed of active devices are replaced by resistive biasing in order to avoid additional noise from bias circuitry.

VCO tuning is realized using accumulation-mode MOS (AMOS) varactors ($C_{\rm var}$). To enhance the Q and reduce the effective $K_{\rm VCO}$, a combination of switched MOS varactors in parallel with a metal-insulator-metal (MIM) capacitor (C_2) is proposed, as illustrated in Fig. 3. Also shown in Fig. 3 is a simplified half-circuit equivalent model of the VCO. The admittance looking from the inductor (L_C) is given by

$$Y_{\rm in} = \frac{1}{R_{\rm buf}} + \frac{1}{R_p} - \frac{C_1 C_{2,\rm eff} g_m \omega^2}{(C_1 + C_{2,\rm eff})^2\omega^2 + g_m^2} + j\omega\left(C_\mu + C_{\rm buf} + \omega^2 \frac{C_1 C_{2,\rm eff}(C_1 + C_{2,\rm eff})}{(C_1 + C_{2,\rm eff})^2\omega^2 + g_m^2}\right). \quad (2)$$

If $g_m \ll (C_1 + C_{2,\rm eff})\omega$, (2) is simplified to

$$Y_{\rm in} = \frac{1}{R_{\rm buf}} + \frac{1}{R_p} - \frac{C_1 C_{2,\rm eff} g_m}{(C_1 + C_{2,\rm eff})^2} + j\omega\left(C_\mu + C_{\rm buf} + \frac{C_1 C_{2,\rm eff}}{C_1 + C_{2,\rm eff}}\right) \quad (3)$$

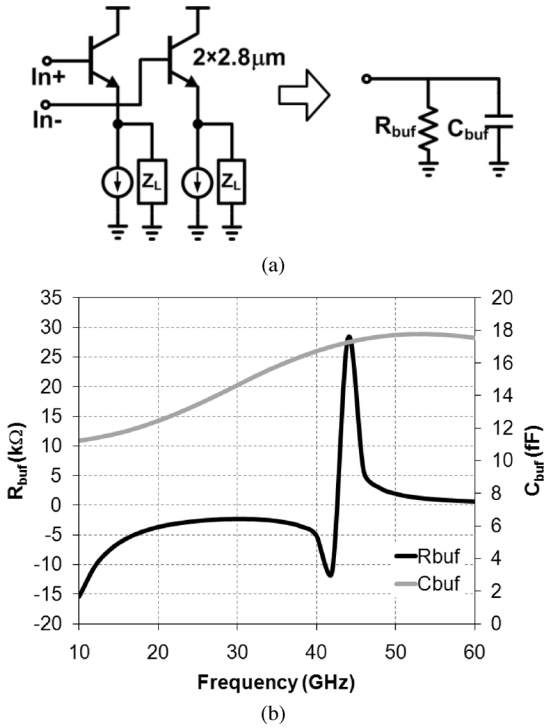


Fig. 4. Emitter follower buffer (a) schematic and (b) simulated input impedance.

where R_p models the inductor loss, $R_{\rm buf}$ and $C_{\rm buf}$ are the equivalent shunt resistance and capacitance of the buffer.

By inspection, the oscillation frequency is

$$\omega_{\rm osc} = \frac{1}{\sqrt{L_C\left[\frac{C_1 C_{2,\rm eff}}{C_1 + C_{2,\rm eff}} + C_\mu + C_{\rm buf}\right]}}. \quad (4)$$

In bipolar design, $R_{\rm buf}$ is a function of the base resistance and frequency. Therefore, care must be taken to co-design the VCO with the buffer. This is because if the real part of the impedance looking into the buffer becomes smaller than the absolute value of the active negative resistance, then the start-up oscillation condition will be compromised. For the Ka-band VCO, a broadband emitter follower is used as the buffer (Fig. 4(a)). Assuming the buffer drives a capacitive load C_L, the effective shunt resistance and capacitance looking into the base are calculated, as follows:

$$R_{\rm buf} = -\frac{(C_\pi + C_L)^2\omega^2 + \left(g_m - C_\pi C_L r_b \omega^2\right)^2}{C_\pi C_L \omega^2 (g_m - C_\pi C_L r_b \omega^2)} \quad (5)$$

$$C_{\rm buf} = \frac{C_\pi C_L (C_\pi + C_L)\omega^2}{(C_\pi + C_L)^2\omega^2 + (g_m - C_\pi C_L r_b \omega^2)^2}. \quad (6)$$

Equation (5) shows a negative input resistance at the buffer input when $g_m > C_\pi C_L r_b \omega^2$. This condition can be met at low-end of mm-wave frequency, as shown in Fig. 4(b). For this design, $R_{\rm buf}$ is made negatively large such that it does not present any loading to the VCO and affect the tank Q. It is noteworthy that this negative resistance provided by the buffer will not affect the oscillation. Therefore, either a negative or a large positive buffer impedance are both viable options.

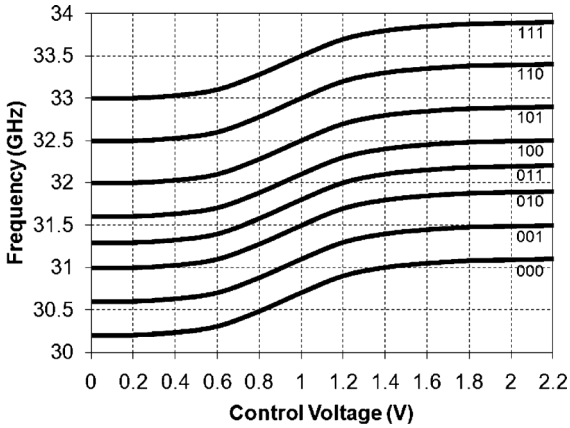


Fig. 5. Measured tuning curves for 32 GHz VCO.

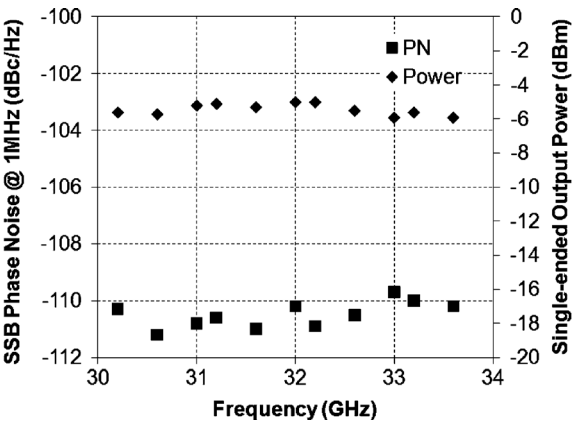


Fig. 6. Measured phase noise and output power.

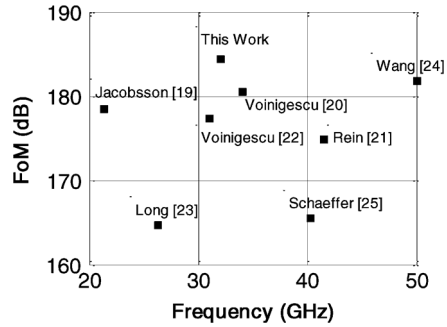


Fig. 7. Comparison with other state-of-the-art VCOs.

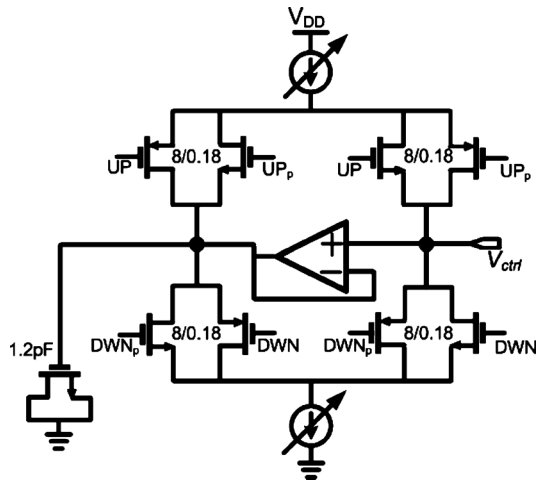


Fig. 8. Simplified schematic of the charge pump.

In designing a differential Colpitts VCO, it is very important to avoid common-mode oscillation. In common-mode, the shunt negative resistance from the emitter follower buffer is still present. Adding resistors at common nodes such as in the degenerated center-tapped inductor (L_d) results in higher common-mode loss, suppressing any common-mode oscillations.

Measurements of the VCO and buffer breakout have been performed on-wafer with an Agilent E4448A spectrum analyzer. The VCO and the buffer consume a total of 35 mW from 2.2 V supply. In Fig. 5, the measured VCO tuning range is 30.2 to 33.9 GHz, corresponding to an 11.5% tuning range. Colpitts topology was chosen since it exhibits low phase noise [17], [18]. The measured phase noise at 1-MHz offset is between -111 and -110 dBc/Hz with an average output power of -5 dBm (Fig. 6). The VCO core consumes 17 mW and the output buffer consumes 18 mW, resulting in an overall FoM ($\mathrm{FoM} = 20\log_{10}(f/\Delta f) - 10\log_{10}(P_{\mathrm{DC}}/1\ \mathrm{mW}) - L\{\Delta f\}$ [19]) of 184.7 dB. Fig. 7 compares the performance of the Colpitts VCO against other state-of-the-art VCOs around the Ka-band frequency.

B. Loop Components: Divider, Phase-Frequency Detector (PFD), Charge Pump (CP), and Loop Filter (LF)

The VCO output signal is fed back through a cascade of divide-by-2 circuits. The first two dividers use emitter-coupled logic (ECL) topologies, while the biasing current is scaled according to the operating frequency. HBTs are biased at peak f_T current density [26], i.e., 8 mA/μm^2. Subsequent divide-by-2 circuits use CMOS CML latches down to 1 GHz frequency, whereafter TSPC dividers are used. This particular order resulted in optimal trade-off between wide frequency locking under PVT variation and power consumption.

The digital PFD is based on a conventional detector [27], and is designed to eliminate the region of low gain near phase lock. The elimination of the dead zone is accomplished by producing an "up" and a "down" current pulses during each cycle, even when the PLL is in lock. Programmable 2-bit delay is added in feedback path for optimal close-in phase noise.

The simplified charge pump cell, shown in Fig. 8, is driven by digital signals UP, DWN, and their complements derived from PFD circuit. Cascode current sources reduce the effect of the VCO control voltage variation on the charge pump UP/DOWN currents until V_{ctrl} comes within $2V_{\mathrm{dsat}}$ of the supply rails. Moreover, the use of cascode current sources reduces the UP/DOWN current mismatch. The use of a dummy branch to steer the charge-pump current for the duration when V_{ctrl} is not integrating any charge, significantly reduces the non-idealities of the charge pump including the charge-injection and clock feed-through cancellation. The common problem of charge sharing in charge pumps is solved by the use of a unity-gain feedback op-amp [28] comprised of a complementary folded cascode amplifier.

For low-cost, the passive 3rd-order loop filter is implemented on-chip. From Fig. 1, C_1 produces the first pole and together with R_1 is used to generate a zero for loop stability. C_2 is used

to smoothen the control voltage ripples. R_3 and C_3 are used to further suppress reference spurs and high frequency noise. The PLL loop has been optimized for a target bandwidth of 1 MHz.

In practice, the inaccuracy of on-chip resistance and capacitance of loop filter and VCO gain affects the PLL bandwidth and phase margin. Therefore, programmable charge pump current and loop filter is designed for PVT variation.

IV. Harmonic Generation

Before discussing the design of active frequency multipliers, it is instructive to study the main source of nonlinearity that generates the wanted harmonics in a bipolar transistor. We will focus our attention on the third harmonic generation, as this is the desired signal for the multiply-by-3 circuit. The HICUM model provided by the foundry is used for the simulation of the HBT device. The two major nonlinearities in the HBT that cause harmonic generation are: (1) the nonlinear exponential I-V characteristic of the HBT, and; (2) the collector current I_C conduction angle and clipping.

The I-V equation of a bipolar transistor can be expressed as [29]

$$i_C = I_S \exp\left(\frac{v_{\rm BE}}{V_t}\right)\left(1+\frac{v_{\rm CE}-v_{\rm BE}}{V_{\rm AF}}\right) = f(v_{\rm BE}) \qquad (7)$$

where I_S, $V_{\rm AF}$ and V_T are the transistor saturation current, the forward early voltage, and the thermal voltage (i.e., $V_T = kT/q$), respectively.

For a given bias ($V_{\rm BE}$) and an input tone ($A\cos(\omega_0 t)$), the third-order harmonic is simply the third-order Fourier component, that is

$$I_3 = \frac{1}{\pi}\int_{-\pi}^{\pi} f(V_{\rm BE}+A\cos(\omega_0 t))\cos(3\omega_0 t)dt \qquad (8)$$

Following the analysis in [30], (8) can be written as

$$I_3 = \frac{2A^3}{5!\times\pi}\int_{-A}^{A}\left(1-\frac{V_{\rm AC}^2}{A^2}\right)^{5/2}\left.\frac{d^3 f(v_{\rm BE})}{dv_{\rm BE}^3}\right|_{V_{\rm BE}+V_{\rm AC}}\frac{dV_{\rm AC}}{A} \qquad (9)$$

where $V_{\rm AC} = A\cos(\omega_0 t)$.

The third-order harmonic is simply an average of the 3rd-order derivative of $f(v_{\rm BE})$ over the input voltage swing with a weighting function $(1-V_{\rm AC}^2/A^2)^{5/2}$. Examining the third derivative of the HBT I-V transfer function, Fig. 9, we see that the main source of nonlinearity of the HBT appears in the regions where the device turns on ($V_{\rm BE} = 0.8$ V), and where the device is near saturation ($V_{\rm BE} > 1$ V). Closer inspection of Fig. 9 reveals that the third derivative can be either positive or negative. Henceforth, depending on the input biasing and swing, there is an optimal point where the average integral in (9) is maximized.

V. Injection-Locked and Harmonic-Based Frequency Tripler

As discussed in Section IV, the design of an active harmonic generator relies on accurate modeling of the transistor itself, proper transistor bias for the specific harmonic required and input fundamental frequency power level. A 0-dBm input power is available from the 32 GHz PLL. Based on this available drive power and simulation of efficiency, defined as $\eta = P_{\rm RF,out}/(P_{\rm DC}+P_{\rm RF,in})$, Fig. 10 shows that the optimal bias voltage leading to maximum efficiency is around 0.82 V, which corresponds to Class AB region. Differential topology was chosen for the multiplier design since it offers seamless integration with the PLL output, higher output power, better linearity, and better even-order harmonic and common-mode rejection. Next, the circuit implementation of this harmonic generator will be discussed in the context of two types of frequency triplers: (1) ILFT and (2) HBFT.

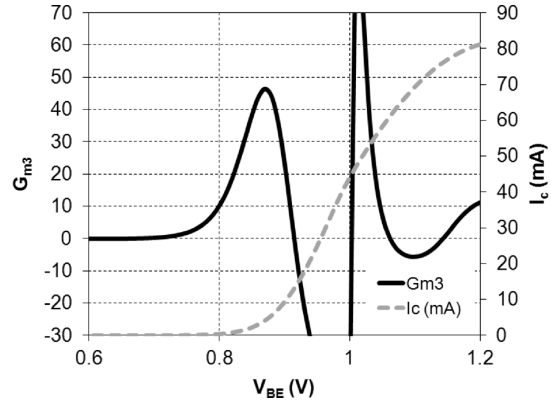


Fig. 9. Simulated SiGe HBT transistor $\rm I_c$ and its third derivative (i.e., $G_{m3} = d^3 I_C/dV_{\rm BE}^3$) as function of $\rm V_{be}$.

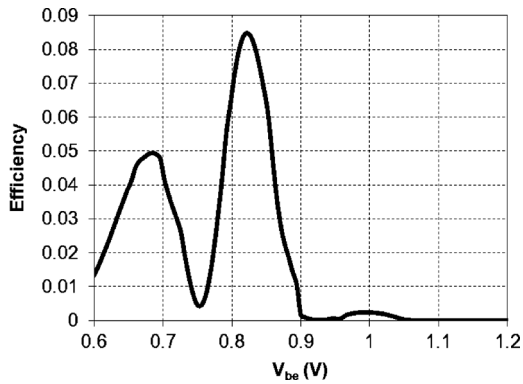


Fig. 10. Simulated efficiency as a function of $\rm V_{be}$.

A. Injection-Locked Frequency Tripler (ILFT)

The schematic of the ILFT is shown in Fig. 11, which consists of two parts: (1) a pair of harmonic generating transistors Q_3&Q_4, and (2) an injection-locked oscillator (ILO). To enable compact layout yet avoid mutual and substrate noise coupling, ground-shielded CPW (G-CPW) lines (T_1-T_3) instead of spiral inductors are used at the base, collector and emitter. The inductance values for T_1, T_2 and $T_3 + L_3$ are 25 pH, 20 pH and 150 pH, respectively. The standalone ILFT has two modes of operation.

Mode 0 (Free-Running Operation): If no signal is applied at the input, the ILFT resembles a conventional common-collector differential Colpitts oscillator. It is commonly assumed that the RF output taken at the collector is isolated from the resonator. However, as will be shown next, due to the Miller effect,[1] the

[1]Small-signal assumption.

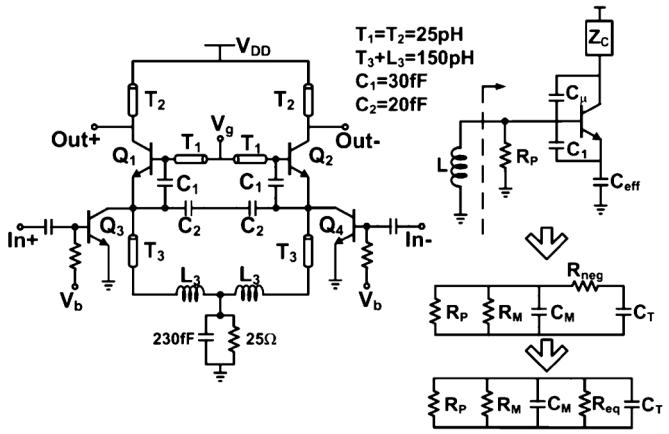


Fig. 11. Schematic and simplified small-signal equivalent circuit of ILFT.

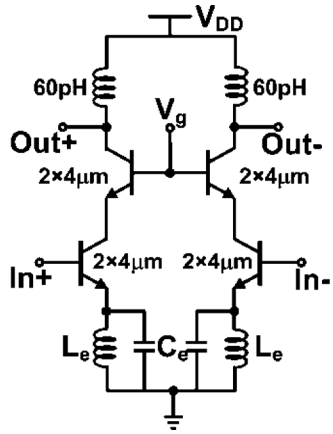


Fig. 12. Schematic of buffer amplifier after ILFT.

parasitic capacitance C_μ reduces the negative resistance and affects the oscillation frequency. Transistors $Q_3\&Q_4$ in Mode 0 act as capacitive degeneration and can be combined with C_2 and T_3+L_3 into an effective capacitor $C_{\rm eff}$. A simplified equivalent circuit used for the derivation of the equivalent input impedance is shown in Fig. 11.

For simplicity, first assume there is no load in the collector, i.e., common-collector. In this configuration, the real part of the input impedance is

$$\begin{aligned}\mathrm{Re}\{Z_{\rm in}\} &= R_{\rm neg} \\ &= -\frac{\frac{g_m}{\omega^2 C_1 C_{\rm eff}}}{\frac{C_\mu^2 g_m^2}{\omega^2 C_1^2 C_{\rm eff}^2}+\left(\frac{C_\mu}{C_1}+\frac{C_\mu}{C_{\rm eff}}+1\right)^2}.\end{aligned} \tag{10}$$

When C_μ approaches zero, $R_{\rm neg}$ reaches a maximum value of $-g_m/(\omega^2 C_1 C_{\rm eff})$, which is the ideal Colpitts negative resistance. When C_μ approaches infinity, $R_{\rm neg}$ becomes zero. Moreover, when C_μ is larger than C_1 and $C_{\rm eff}$, the negative resistance will be inversely proportional to C_μ^2. In (10), we assume the collector is at AC ground. Next, we will examine the C_μ effect on the tank for a load impedance Z_C at the collector of Q_1-Q_2.

Fig. 11 shows the equivalent circuit seen at the input considering C_μ. Z_M (defined as $Z_M = R_M\|1/(C_M s)$) is the effective Miller impedance seen at the base, i.e., $Z_M = Z_{\rm bc}(1-A_v)$, where A_v is the base-collector voltage gain and is given by

$$\frac{V_o}{V_i} = A_V = -\frac{g_m Z_C}{1+\frac{C_1}{C_{\rm eff}}+\frac{g_m}{j\omega C_{\rm eff}}}. \tag{11}$$

Z_C can be inductive, resistive (at the resonant frequency), or capacitive. For a purely inductive load, $Z_C = j\omega L_C$, it is shown in Appendix that

$$\begin{aligned}R_M &= \frac{-1}{\omega C_\mu \mathrm{Im}(1-A_V)} = -\frac{g_m^2+\omega^2(C_1+C_{\rm eff})^2}{g_m L_C C_{\rm eff} C_\mu \omega^4 (C_1+C_{\rm eff})} \\ &\approx -\frac{g_m}{L_C C_{\rm eff} C_\mu \omega^4 (C_1+C_{\rm eff})}\end{aligned} \tag{12}$$

$$\begin{aligned}C_M &= C_\mu \mathrm{Re}(1-A_V) \\ &= C_\mu\left[1-\frac{\omega^2 L_C C_{\rm eff}}{1+\omega^2(C_1+C_{\rm eff})^2/g_m^2}\right].\end{aligned} \tag{13}$$

Next, if the tank loss (in the form of parallel R) is taken into account, $Z_C = j\omega L_C R/(R+j\omega L_C)$, then

$$\begin{aligned}R_M &= -\frac{\left(g_m^2+\omega^2(C_1+C_{\rm eff})^2\right)\left(1+\frac{\omega^2 L_C^2}{R^2}\right)}{\frac{C_{\rm eff} C_\mu g_m^2 L_C^2 \omega^4}{R}+g_m L_C C_{\rm eff} C_\mu \omega^4 (C_1+C_{\rm eff})} \\ &\approx -\frac{g_m^2\left(1+\frac{1}{Q^2}\right)}{\frac{C_{\rm eff} C_\mu g_m^2 L_C \omega^3}{Q}+g_m L_C C_{\rm eff} C_\mu \omega^4 (C_1+C_{\rm eff})}.\end{aligned} \tag{14}$$

From (12) and (14), a higher L_C increases the output power, but reduces the effective negative resistance, necessitating higher power consumption from the oscillator core. From (14), higher inductor Q leads to higher R_M.

To guarantee oscillation, the resultant resistance $R_p\|R_M\|R_{\rm eq}$ must be negative, which implies $|R_M\|R_{\rm eq}| < R_p$, where $R_{\rm eq}$ is

$$R_{\rm eq} = -\frac{(C_1+C_{\rm eff})^2\omega^2+g_m^2}{C_1 C_{\rm eff} g_m \omega^2}. \tag{15}$$

Therefore, at high frequencies approaching the transistor f_T, i.e., lower g_m and the high base-to-collector capacitance, the effect of the collector load on the tank becomes significant, leading to smaller negative resistance. As in the case of 32 GHz VCO, common-mode oscillation must be avoided by quenching all high Q common-mode nodes.

To further guarantee sufficient negative resistance margin for oscillation start-up, the buffer that follows the ILFT is an inductively peaked cascode, employing capacitive degeneration to increase the input base impedance and mitigate the loading effects through the Miller effect on the tank. Fig. 12 shows the buffer where the degeneration $L_e = 50$ pH and $C_e = 90$ fF resonates lower than the operation frequency of the tripler, i.e., 96 GHz. The simulated effect of capacitor degeneration on the real part of the small-signal input impedance looking into the tank (including inductor loss R_p) is shown in Fig. 13. It clearly displays the improvement in small-signal negative resistance as a result of capacitor degeneration.

Mode 1 (Input @ Subharmonic $\omega_0/3$): Injection-locking operation is realized by feeding the 3rd harmonic of the input signal generated by $Q_3\&Q_4$ into the tank of the ILO. Transistors $Q_3\&Q_4$ re-use part of the DC current of the VCO and are

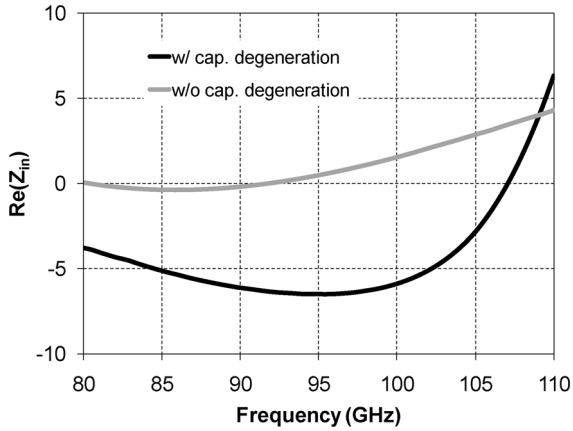


Fig. 13. Simulated small-signal input negative resistance of ILFT with the buffer loading with and without capacitive degeneration.

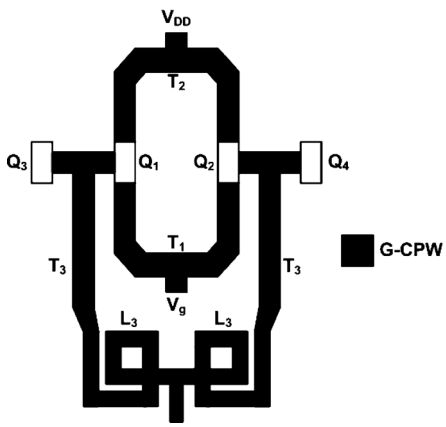


Fig. 14. Simplified layout floorplan of the ILFT (not to scale).

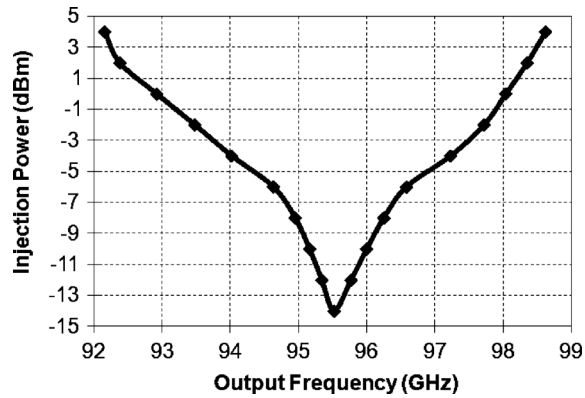


Fig. 15. Measured input sensitivity of ILFT breakout.

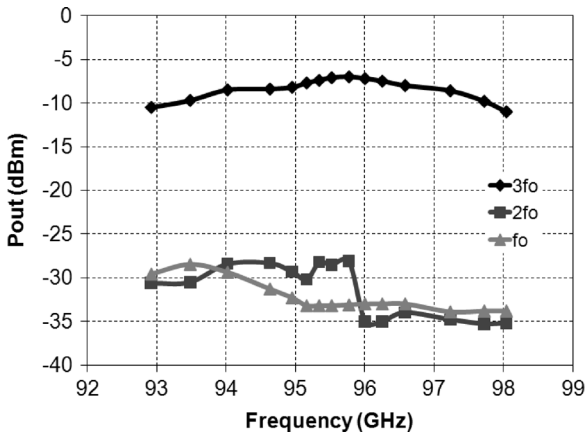


Fig. 16. Measured breakout of ILFT output power of harmonic across frequency.

biased in Class-AB regime for maximum efficiency of 3rd harmonic generation, as described in Section IV. From injection locking theories [31], if phase error exists between the oscillator and the injection locking signals, the *LC* tank of the oscillator would create an additional phase shift to ensure the oscillation phase condition is satisfied. Using Adler's equation [32], the locking range is given by

$$\omega_L \leq \frac{\omega_o}{2Q}\sqrt{\frac{I_3^2}{I_o^2+I_3^2}} \approx \frac{\omega_o}{2Q}\left|\frac{I_3}{I_o}\right| \tag{16}$$

where Q represents the quality factor of the tank, I_3 and I_o are the third-harmonic injection and oscillator currents. From (16), the locking range is strongly influenced by the harmonic generator bias, which generates the desired I_3. Although adding varactors to the tank helps improve the locking range by varying the self-oscillation frequency, no varactors are used in this design since neither AMOS nor HBT varactors has a Q factor larger than 3 at 96 GHz in the given technology. However, since HBT transistors exhibit much stronger nonlinearity compared to MOS transistors due to its inherently exponential I-V relationship, a wide locking range can still be achieved without varactor tuning. The layout floorplan for the proposed ILFT is shown in Fig. 14. To enable compact layout yet avoid mutual and substrate noise coupling, ground-shielded CPW (G-CPW) lines ($T_1 \sim T_3$) [33] are used at base, collector, and emitter to provide the tank, the load, and part of the degeneration inductances. Additional emitter degeneration inductance is realized by spiral inductor (L_3) to save area. The G-CPW structure is favored because it can realize small inductance with good modeling accuracy and adequate Q factor. The tank and load inductors ($T_1\&T_2$) are the most critical ones, which are placed as close as possible to the core transistors ($Q_1\&Q_2$ in Fig. 11), but on opposite sides. All inductors are realized by G-CPW with M6 as the top metal and M1 as ground shield. In order to match the degeneration inductor with the core layout, part of its inductance is realized using G-CPW. Note that ILFT is susceptible to injection-pulling when used in a system. Fortunately, G-CPW minimizes coupling among the tank, load, and degeneration inductors and also shields from the substrate.

It is well known that an ILO is equivalent to a first order PLL [34], where input phase noise is lowpass filtered and oscillator phase noise is high pass filtered. If $S_{\rm PLL}$ is the phase noise of the injected signal, $S_{\rm harm}$ is the phase noise of the harmonic amplifier, and $S_{\rm OSC}$ is the oscillator phase noise, then the phase noise of the ILFT can be expressed as [35]

$$S_{\rm out,ILFT}(\Delta\omega) = \frac{3^2}{1+\left(\frac{\Delta\omega}{\omega_L}\right)^2}S_{\rm PLL}(\Delta\omega) + \frac{1}{1+\left(\frac{\Delta\omega}{\omega_L}\right)^2}S_{\rm harm}(\Delta\omega) + \frac{\left(\frac{\Delta\omega}{\omega_L}\right)^2}{1+\left(\frac{\Delta\omega}{\omega_L}\right)^2}S_{\rm OSC}(\Delta\omega). \tag{17}$$

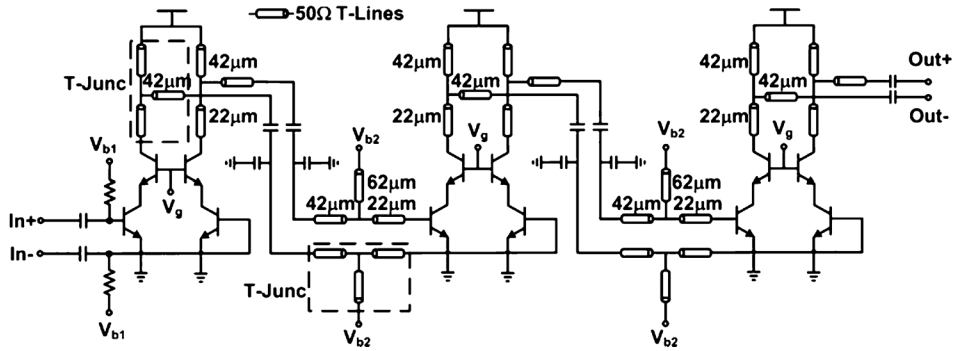


Fig. 17. Simplified schematic of harmonic frequency tripler.

It can be seen from (17)[2] that the output phase noise near the carrier is dominated by the injected signal plus additional degradation from the harmonic generator. At the offset frequency $\Delta\omega$ far from the carrier, the phase noise of the ILFT is that of the oscillator phase noise. The tank Q can thus be relaxed to improve the ILO locking range at the expense of degradation in the integrated phase noise. In other words, the ILO can be designed for tuning range, as its output phase noise is primarily determined by the phase noise of the injected signal. Note that the tank Q also affects the oscillator's small-signal negative resistance. Therefore, care must be taken to ensure sufficient margin for oscillation.

A breakout circuit of the ILFT is separately fabricated and characterized. The free-running frequency is 95.5 GHz. Fig. 15 shows the measured input sensitivity curve of ILFT. For 0 dBm input power the locking range is 92.8–98.1 GHz, which is sufficient for imaging applications [1]. The measured single-ended output power versus frequency is shown in Fig. 16 for a 0 dBm input power with fundamental suppression of >22 dB below the desired third harmonic output. It can be expected that for balanced outputs, the second harmonics will be reduced. The tripler and buffer circuits consume 75 mW from 2.5 V supply.

B. Harmonic Balance Frequency Tripler (HBTF)

The architecture of the HBFT is shown in Fig. 17. It consists of three stages: the harmonic generation stage, which converts a 32 GHz input signal to 96 GHz, followed by two LO amplification and filtering stages working at 96 GHz. All three stages adopt the pseudo-differential cascode topology. Again, the first stage transistor is biased at optimum 3rd-harmonic efficiency bias voltage. In contrast, the latter two stages are biased in Class-A region. In a symmetric design of a differential amplifier, the even harmonics of the collector currents appear as common mode components and should cancel out in the differential output voltage. The amplifier's load is tuned to the third harmonic to maximize the gain at 96 GHz and suppress all other harmonics. Interstage matching is achieved using MIM capacitors and 50 Ω G-CPW t-lines. The simulated differential impedance looking into the collector is 17-$j72$ Ω, p_1 on the Smith Chart (normalized to 100 Ω) in Fig. 17, and is matched to 100 Ω impedance using a G-CPW T-junction, p_2, and a series MIM capacitor. For the input matching, starting from the 100 Ω input, a shunt MIM capacitor moves the impedance to p_3. The matching is finalized with a different length G-CPW T-junction, p_4, to 23-$j12$ Ω input impedance of the transistor. Fig. 18 illustrates the matching procedure on the Smith Chart.

[2]Note that (17) holds true if the injected signal's frequency is near the ILFT free running frequency and deviates from it when the input frequency is away from the center of the locking range as shown in [31].

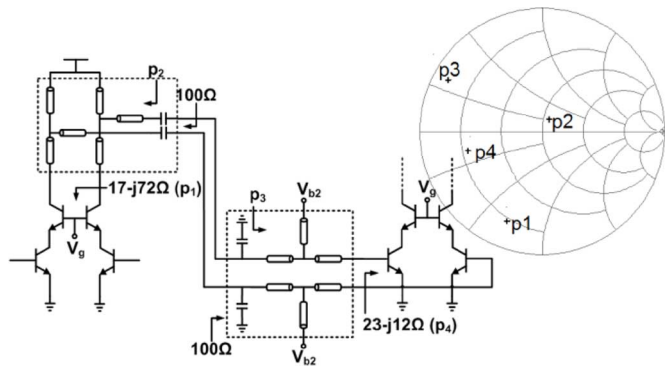


Fig. 18. Interstage matching procedure in HBFT.

For the HBFT, the multiplier and amplifier chain can impart phase noise in addition to the minimum $20\log(3)$ dB degradation. Using a linear phase model [36], we can express the output phase noise of HBFT as

$$S_{\mathrm{out,HBFT}}(\Delta\omega) = 3^2 S_{\mathrm{PLL}}(\Delta\omega) + S_{\mathrm{harm}}(\Delta\omega) + S_{\mathrm{amp}}(\Delta\omega). \tag{18}$$

Unlike the ILFT, the HBFT does not resemble a PLL, so noise from the harmonic generator stage and two-stage amplifier can increase the integrated phase noise. Typically, amplifier's noise contribution is lower than the oscillator. Therefore, S_{PLL} dominates (18). The simulated $\mathrm{OP}_{1-\mathrm{dB}}$ of the cascaded amplifier is -2 dBm. Amplifiers following the multiplier do not suffer multiplication by 3^2. Again, assuming the amplifier operates in the linear region, its phase noise is a function of the input power and noise figure [36]. Therefore, the noise level of amplifier stages after the multiplier is kept low by biasing the first stage at minimum NF current density, whereas the second stage is biased for maximum f_{MAX}.

A breakout circuit of the HBFT is also fabricated and measured separately. Fig. 19 presents the frequency response of the circuit. The tripler achieves an output power of -10 dBm and a 3-dB bandwidth of 20 GHz for an input power of 0 dBm. The measurements show that the first and second harmonics are suppressed more than 20 dB compared to the desired third

TABLE I
PERFORMANCE COMPARISON OF MILLIMETER-WAVE ACTIVE MULTIPLIERS

	Lin MWCL'09 [37]	Heydari IMS'10 [38]	Wang TMTT'11 [39]	Long ISSCC'08 [40]	This work ILFT	This work HBFT
Type	Harmonic×2	IL×3	Harmonic×3	IL×3	IL×3	Harmonic ×3
Frequency	66GHz	93GHz	60GHz	60GHz	96GHz	90GHz
Bandwidth/ Locking Range	12%	6%	10.5%	13.3%	5.5%	22%
Conversion Gain (dB)	10.2	-6	-1.6	-27	-7	-10.5
Output Power (dBm)	1.7	-7	-2.6	-27	-7	-10.5
Input Power (dBm)	-8.5	-1	-1	0	0	0
Harmonic Rejection	>30dBc	-	>15dBc	-	>20dBc	>20dBc
Supply (V)	2.5	1.0	1.2	1.0	2.5	2.5
Power (mW)	137	19.8	56	23.8	75	75
Technology	0.18μm SiGe BiCMOS	65nm CMOS	0.15μm PHEMT	90nm CMOS	0.18μm SiGe BiCMOS	0.18μm SiGe BiCMOS

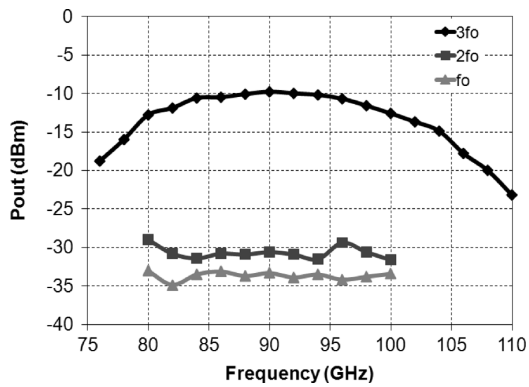
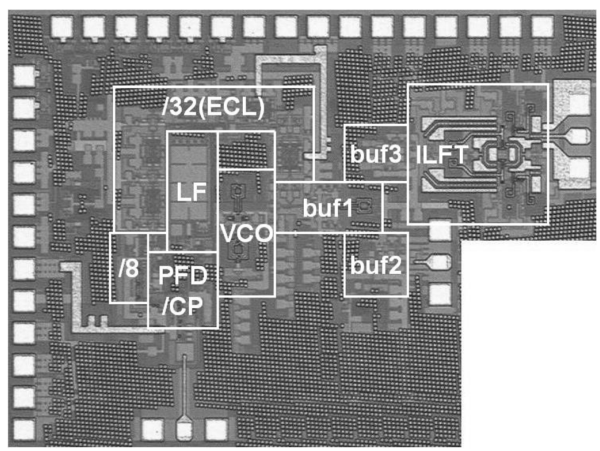
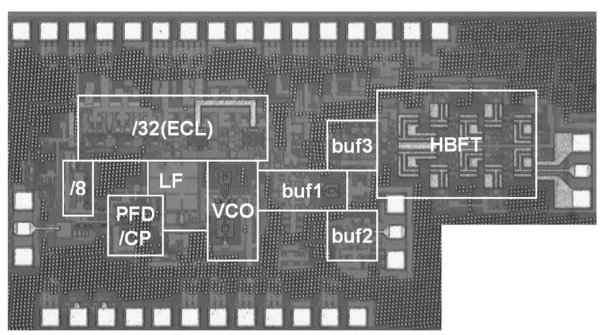


Fig. 19. Measured breakout of HBFT output power of harmonic across frequency.



(a)



(b)

Fig. 20. Die photo of (a) PLL with ILFT (Chip A) and (b) PLL with HBFT (Chip B).

harmonic. Again, for a differential output, the second harmonic should be suppressed further. The harmonic stage and subsequent two-stage driver amplifiers consume 5 mW and 70 mW, respectively, under a 2.5 V supply. Table I provides a performance comparison of mm-wave active multipliers.

VI. EXPERIMENTAL RESULTS

The two chips have been fabricated in a 0.18 μm SiGe BiCMOS process with six metal layers. The emitter width of the HBTs in the technology is 0.15 μm. Fig. 20(a) and (b) show die micrographs of the PLL-ILFT (1.8 mm^2) and the PLL-HBFT (1.9 mm^2) frequency synthesizers, respectively. The chip area can be further reduced, as two of the three buffers are included for test purposes only.

The 2.8 μm-thick top metal is used to realize inductors and t-lines in mm-wave circuits, i.e., VCO, ILFT and HBFT. Signal distribution and routing between building blocks has been accomplished carefully using the 1.6 μm-thick penultimate metal layer (M5) to minimize coupling to the oscillator tanks in the top-metal layer. Since G-CPWs can provide excellent isolation between adjacent circuits, they were adopted in the design of ILFT and HBFT. All passives including MIM capacitors and interconnects, used in the PLL, have been designed or characterized using planar 3-D electromagnetic simulations [41].

The frequency synthesizer chip is attached to a PCB using chip-on-board assembly. All DC pads are wirebonded to the PCB. The reference frequency input is provided by an on-board 125 MHz voltage controlled crystal oscillator (VCXO). With the PCB mounted on a probe station, the chip performance is

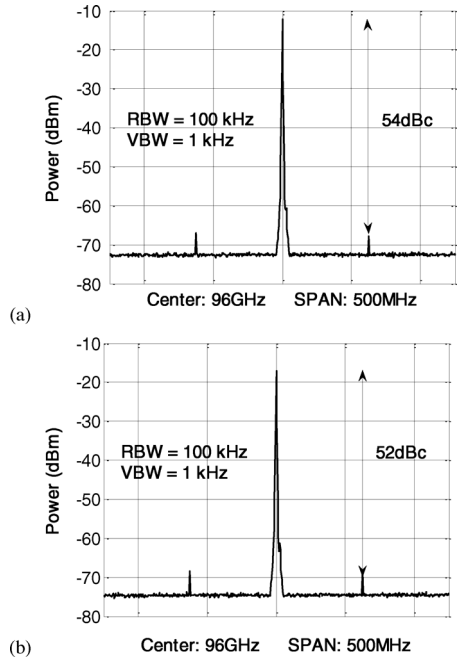


Fig. 21. Measured output spectra of (a) PLL + ILFT and (b) PLL + HBFT.

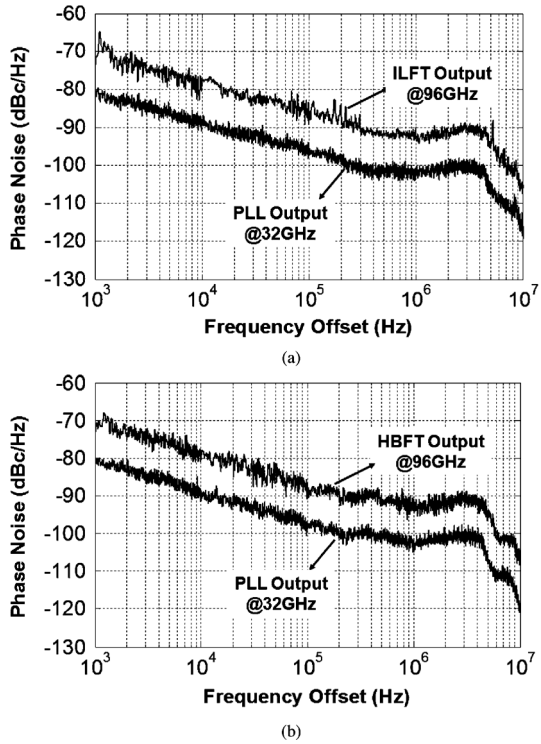


Fig. 22. Measured phase noise of (a) PLL + ILFT and (b) PLL + HBFT.

characterized by on-wafer measurements. The 32 GHz mode is measured using a simple coaxial setup. A WR-10 waveguide-based setup is used for the 96 GHz mode including an Agilent 11970 W harmonic mixer.

The single ended 96 GHz output spectra measured at the output of the ILFT and the HBFT are shown in Fig. 21(a) and (b), respectively (measurement loss not de-embedded). Both chips achieve reference spurs better than 52 dBc. The core PLL achieves a measured tuning range of 30.3–33.8 GHz and delivers an average differential output power of 0 dBm. Chip A achieves a tuning range of 92.8–98.1 GHz, which is limited by the locking range of the ILFT. For Chip B, the measured tuning range is 90.9–101.4 GHz, which is three times the PLL tuning range.

PLL-based frequency multipliers' phase noise are important properties of the transceiver's LO performance. This is particularly true of transceivers used in phase-modulated communication systems, because the phase noise of the receiver/transmitter LO is transferred degree-for-degree to the received/transmitted signal [42]. The closed-loop phase noise profiles of both chips are depicted in Fig. 22(a) and (b).

The phase noise of the core PLL is also plotted in the same figure. The phase noise at 1 MHz offset measured at the output of the PLL, ILFT and HBFT are -103 dBc/Hz, -93 dBc/Hz, and -92 dBc/Hz, respectively. The phase noise at 96 GHz roughly scales by $20\log(3)$ from the 32 GHz output of the core PLL.

Figs. 23(a) and (b) summarizes the phase noise of synthesized frequencies at 1 MHz offset. A plot of the measured 100 kHz to 100 MHz RMS phase noise across the synthesized output is also shown. The average RMS phase noise for chip A is 5.4° for an integration bandwidth from 100 kHz to 100 MHz, whereas for chip B is 5.5°. These phase noise measurements verify that in a synthesizer incorporating a low phase noise subharmonic PLL followed by an ILFT or an HBFT, the residual increase in phase noise is less than a typical degradation seen in a W-band fundamental PLL [7].

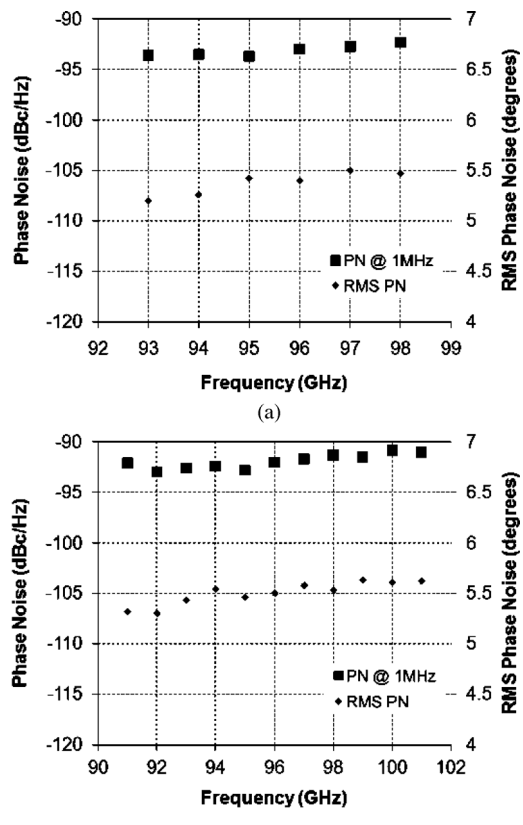
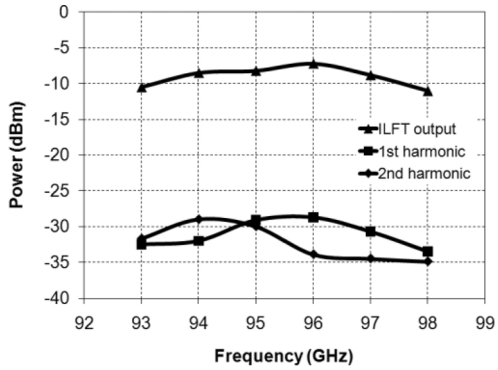
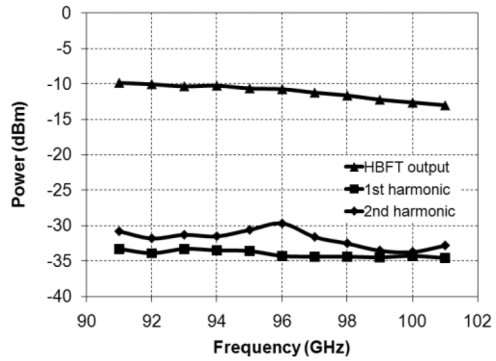


Fig. 23. Measured phase noise and RMS jitter of (a) PLL + ILFT and (b) PLL + HBFT.



(a)



(b)

Fig. 24. Measured output frequency response of (a) PLL + ILFT and (b) PLL + HBFT.

TABLE II
PERFORMANCE SUMMARY

		PLL+ILFT (Chip A)	PLL+HBFT (Chip B)
Frequency Range	Core PLL	30.3-33.8GHz	30.3-33.8GHz
	Output Frequency	92.8 to 98.1GHz	90.9 to 101.4GHz
Reference Frequency		125MHz	125MHz
PLL Loop Bandwidth		1MHz	1MHz
Power Consumption		140mW	140mW
Phase Noise @ 1MHz offset		-92.3 to -93.7dBc/Hz	-90.8 to -93dBc/Hz
RMS Phase Noise (100kHz-100MHz)		5.3 to 5.5 degrees	5.4 to 5.6 degrees
Spurious emissions	Reference spur	-55 to -52dBc	-53 to -50dBc
	1st harmonic	-25 to -23dBc	-23 to -20dBc
Die Size		1.8mm²	1.9mm²
Technology		0.18μm SiGe BiCMOS	0.18μm SiGe BiCMOS

Fig. 24 shows the power of the single-ended output signal and power of the major harmonics for output signals after ILFT (Chip A) and HBFT (Chip B). The measured signal output power is around -7 dBm and -11 dBm over the bandwidth for Chip A and B, respectively. The largest spur is due to the feed-through of the core PLL. Again, it can be expected that for differential output the second harmonic will be reduced at the output. Suppression for the first and second harmonics are observed to be better than 20 dB compared to the triplers' output for both chips.

Finally, Chip A has been verified in a multi-channel system [1]. The core PLL consumes 65 mW, and both the ILFT and the HBFT consume 75 mW. The measured performance of the 96 GHz synthesis is summarized in Table II.

VII. Comparison Between Chip A and B

Based on the measurement results of the two prototypes, three different methods for W-band frequency synthesis were compared in terms of phase noise, tuning range, and output power. The first two methods are based on the performance of Chip A and Chip B. The third method involves a fundamental 96 GHz PLL. For ease of comparison, both the ILFT and the HBFT are designed with same power consumption. Note that the power consumption of both Chip A and Chip B should be similar to that of a 96 GHz PLL, because the reduced power consumption in the divider is offset by the additional power in the multiplier.

For ideal frequency scaling, as frequency triples, the absolute tuning range also increases by a factor of three and phase noise degrades by 9.54 dB $(20\log_{10} 3)$. However, mm-wave fundamental oscillators generally suffer from narrower tuning range due to the impact of large fixed parasitic capacitance to the overall tank capacitance. Also, the impact of noise sources from both active and passive devices is exacerbated at higher frequencies and generally more than 9.54 dB phase noise degradation is observed. These assertions are corroborated in recent publications in both CMOS [7] and SiGe BiCMOS [5], [43] and [44].

Chip B degrades the phase noise by 11 dB and triples the tuning range, i.e., it maintains the same fractional tuning range. The tuning range of Chip A is limited by the locking range of ILFT which is dependent on the injection power, and the phase noise degradation is 10 dB. Assuming the use of commercial crystal oscillator in the range of 200 MHz and a fixed PLL bandwidth in the range of few MHz, a fundamental PLL will see a higher phase noise compared to either Chip A or B. Moreover, Chip A has better RMS phase noise than Chip B since at an offset frequency above 10 MHz the amplifier noise after the harmonic generation starts to dominate and two-stage amplifier is noisier than one stage. Furthermore, the output power of the ILO is higher than the output power of the harmonic amplifier, reducing the phase noise impact of latter stages.

Since the ILFT in Chip A is not in the PLL loop there is no guarantee that the tripler is actually locked to the output of the PLL. Hence, this architecture is more suitable for applications that require narrow LO tuning range such as passive imaging [1]. So compared to Chip A, the use of HBFT in Chip B as an open loop harmonic amplifier enables wide LO tuning range limited only by the PLL locking range.

In terms of output power, Fig. 25 plots $\mathrm{P_{out}}$ versus $\mathrm{P_{in}}$ measured from the breakouts of ILFT and HBFT. The ILFT output has less dependency on the input power above -4 dBm. Even for input power below -4 dBm, the output degrades only by 2–3 dB. On the other hand, the HBFT output is highly dependent on $\mathrm{P_{in}}$. The results indicate that the ILFT is more energy efficient, and is capable of providing good output power even when input power is low.

VIII. Conclusion

Two highly integrated 96 GHz frequency synthesis prototypes (Chip A and B) have been designed and implemented in a 0.18 μm SiGe BiCMOS. Both chips exhibit good phase noise and harmonic suppressions and consume same amount of power, while the main trade-off is between tuning range and output power. Table III compares Chip A and B with other

TABLE III
PERFORMANCE COMPARISON OF W-BAND PLLS

	Lee JSSC'08 [11]	Voinigescu JSSC'11 [5]	Chang RFIC'10 [10]	Liu ISSCC'09 [8]	This work PLL+ILFT	This work PLL+HBFT
Center freq.	75GHz	89GHz	74GHz	96GHz	96GHz	96GHz
Type	Fundamental	Fundamental	Fundamental	Fundamental	Subharmonic	Subharmonic
Divide Ratio	32	16,32,64, 128	1024~ 1984	256	256***	256***
Reference Frequency	2.34GHz	5.63GHz* 703MHz**	68.4MHz	375MHz	125MHz	125MHz
Loop Bandwidth	2.5MHz	1.72MHz** 5.4MHz*	300kHz	2MHz	1MHz	1MHz
Tuning range	0.43%	6.7%	10.8%	1.5%	5.5%	10.9%
PN @1MHz	-92dBc/Hz	-98dBc/Hz* -82dBc/Hz**	-83dBc/Hz	-76dBc/Hz	-93dBc/Hz	-92dBc/Hz
Reference Spurs	<-72dBc	N/A	-49dBc	-51.8dBc	-54dBc	-52dBc
Supply (V)	1.45	2.5/1.8	1.0	1.2	2.5/1.8	2.5/1.8
Power (mW)	88	550	65	43.7	140	140
Technology	90nm CMOS	0.13μm SiGe BiCMOS	65nm CMOS	65nm CMOS	0.18μm SiGe BiCMOS	0.18μm SiGe BiCMOS

*Using /16 divider ratio ***Divider ratio of the 32GHz PLL

**Using /128 divider ratio

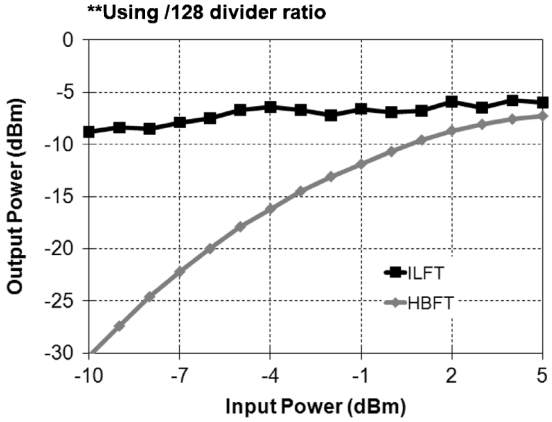


Fig. 25. Measured output power at 96 GHz against input power at 32 GHz for ILFT and HBFT.

state-of-the-art W-band PLLs. Based on the measurement results and analytical studies, the benefits of using a subharmonic PLL followed by a frequency tripler were discussed and highlighted. The work demonstrates further that single-chip W-band synthesizers could be realized with the help of high performance lower frequency PLL. This frequency synthesis is applicable to a broad range of mm-wave systems, from phased arrays to multi-pixels systems.

APPENDIX

The amplifier base-collector voltage gain is given by

$$\frac{V_o}{V_i} = A_V = -\frac{g_m Z_L}{1 + \frac{C_1}{C_2} + \frac{g_m}{j\omega C_2}} \tag{A1}$$

where Z_L is collector load impedance. If Z_L is a parallel *RLC* network, the effective impedance can be inductive, resistive or capacitive, depending on whether the operating frequency is lower than, equal to or higher than the *LC* resonant frequency.

For $\omega < \omega_o$, assume a purely inductive load $Z_L = j\omega L$

$$\mathrm{Re}(1 - A_V) = \frac{g_m^2\left(1 - \omega^2 LC_2\right) + \omega^2(C_1 + C_2)^2}{g_m^2 + \omega^2(C_1 + C_2)^2} \tag{A2}$$

$$\mathrm{Im}(1 - A_V) = \frac{g_m LC_2\omega^3(C_1 + C_2)}{g_m^2 + \omega^2(C_1 + C_2)^2} \tag{A3}$$

then the Miller impedance, Z_M, can be transformed into equivalent parallel resistance and capacitance, R_M and C_M as follows:

$$\begin{aligned} R_M &= \frac{-1}{\omega C_\mu \mathrm{Im}(1 - A_V)} = -\frac{g_m^2 + \omega^2(C_1 + C_2)^2}{g_m LC_2 C_\mu \omega^4 (C_1 + C_2)} \\ &\approx -\frac{g_m}{LC_2 C_\mu \omega^4 (C_1 + C_2)} \end{aligned} \tag{A4}$$

$$\begin{aligned} C_M &= C_\mu \mathrm{Re}(1 - A_V) \\ &= C_\mu \frac{g_m^2\left(1 - \omega^2 LC_2\right) + \omega^2(C_1 + C_2)^2}{g_m^2 + \omega(C_1 + C_2)^2}. \end{aligned} \tag{A5}$$

If tank loss is taken into account, $Z_L = j\omega LR/(R + j\omega L)$, then

$$\mathrm{Im}(1 - A_V) = \frac{C_2 g_m^2 L^2 R\omega^3 + g_m LC_2 R^2 \omega^3 (C_1 + C_2)}{\left(g_m^2 + \omega^2(C_1 + C_2)^2\right)\left(R^2 + \omega^2 L^2\right)} \tag{A6}$$

and

$$\begin{aligned} R_M &= -\frac{\left(g_m^2 + \omega^2(C_1 + C_2)^2\right)\left(1 + \frac{\omega^2 L^2}{R^2}\right)}{\frac{C_2 C_\mu g_m^2 L^2 \omega^4}{R} + g_m LC_2 C_\mu \omega^4 (C_1 + C_2)} \\ &= -\frac{\left(g_m^2 + \omega^2(C_1 + C_2)^2\right)\left(1 + \frac{1}{Q}\right)}{\frac{C_2 C_\mu g_m^2 L\omega^3}{Q} + g_m LC_2 C_\mu \omega^4 (C_1 + C_2)}. \end{aligned} \tag{A7}$$

For $\omega > \omega_o$, assume a purely capacitive load $Z_L = (1)/(j\omega C)$

$$\mathrm{Re}(1-A_V) = \frac{g_m^2(C+C_2)+\omega^2 C(C_1+C_2)^2}{C\left(g_m^2+\omega^2(C_1+C_2)^2\right)} \quad \text{(A8)}$$

$$\mathrm{Im}(1-A_V) = -\frac{g_m C_2\omega(C_1+C_2)}{C\left(g_m^2+\omega^2(C_1+C_2)^2\right)}. \quad \text{(A9)}$$

Again the Miller impedance, Z_M, can be decomposed into equivalent R_M and C_M

$$\begin{aligned} R_M &= \frac{-1}{\omega C_\mu \mathrm{Im}(1-A_V)} \\ &= \frac{C\left(g_m^2+\omega^2(C_1+C_2)^2\right)}{g_m C_2 C_\mu \omega^2(C_1+C_2)} \\ &\approx \frac{C g_m}{C_2 C_\mu \omega^2(C_1+C_2)} \end{aligned} \quad \text{(A8)}$$

$$\begin{aligned} C_M &= C_\mu \mathrm{Re}(1-A_V) \\ &= C_\mu \frac{g_m^2(C+C_2)+\omega^2 C(C_1+C_2)^2}{C\left(g_m^2+\omega^2(C_1+C_2)^2\right)}. \end{aligned} \quad \text{(A9)}$$

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Chun-Cheng Wang (S'07) received the B.S. and M.Eng. degrees in electrical and computer engineering from Cornell University, Ithaca, NY, in 2003 and 2004, respectively.

From 2004 to 2007 he was with Realtek Semiconductor Corporation as an Analog/RF Design Engineer, where he was involved in the design of 802.11 a/b/g/n CMOS radio. He is currently working toward the Ph.D. degree in electrical engineering at University of California, Irvine. His research interests are in RF and millimeter-wave (mm-wave) integrated circuit design for wireless communications, automotive radars, and imaging applications. During his Ph.D., he interned at Fujitsu Laboratories of America, Sunnyvale, CA and Broadcom Corp., Irvine, CA, both involved in the design of 60 GHz CMOS radio.

Mr. Wang was the recipient of the Mindspeed Fellowship in 2011, the Center of Pervasive Communications and Computing (CPCC) Fellowship Award in 2010, the School of Engineering Research and Travel Grant Award in 2009 and the EECS Department Fellowship in 2007 at University of California, Irvine. He is a member of Golden Key Honor Society and Eta Kappa Nu.

Zhiming Chen (S'08) received the B.Eng. degree in electronic engineering from Tsinghua University, Beijing, China, in 2007, and the M.S. degree in electrical engineering from the University of California, Irvine, in 2009, where he is currently pursuing the Ph.D. degree in electrical engineering.

He has been with the Nanoscale Communication IC Laboratory, University of California, Irvine, since 2007. He was a summer intern at Finisar Corporation, Sunnyvale, CA, in 2008. He has been an intern at Broadcom Corporation since June 2010, where he was engaged in 60 GHz phased-array radio development. His research interests include RF/MMW integrated circuits design with a focus on W-band imaging systems.

Payam Heydari (S'98–M'00–SM'07) received the B.S. and M.S. degrees (hons.) in electrical engineering from the Sharif University of Technology, Tehran, Iran, in 1992 and 1995, respectively. He received the Ph.D. degree in electrical engineering from the University of Southern California in 2001.

In August 2001, he joined the University of California, Irvine, where he is currently a Professor of electrical engineering. His research interests include the design of high-speed analog, radio-frequency (RF), and mixed-signal integrated circuits. He is the (co)-author of one book and more than 90 journal and conference papers.

Dr. Heydari was named one of 10 outstanding innovators at the university by the The Office of Technology Alliances at UCI. He is the co-recipient of the 2009 Business Plan Competition First Place Prize Award and Best Concept Paper Award both from Paul Merage School of Business at UC-Irvine. He is the recipient of the 2010 Faculty of the Year Award from UC-Irvine's Engineering Student Council (ECS), the 2009 School of Engineering Fariborz Maseeh Best Faculty Research Award, the 2007 IEEE Circuits and Systems Society Guillemin–Cauer Award, the 2005 NSF CAREER Award, the 2005 IEEE Circuits and Systems Society Darlington Award, the 2005 UCI's School of Engineering Teaching Excellence Award, the Best Paper Award at the 2000 IEEE International Conference on Computer Design (ICCD), the 2000 Honorable Award from the Department of EE-Systems at the University of Southern California, and the 2001 Technical Excellence Award in the area of Electrical Engineering from the Association of Professors and Scholars of Iranian Heritage (APSIH). He was recognized as the 2004 Outstanding Faculty at the UCI's EECS Department. His research on novel low-power multi-purpose multi-antenna RF front-ends received the Low-Power Design Contest Award at the 2008 IEEE Int'l Symposium on Low-Power Electronics and Design (ISLPED). He is the co-founder of ZeroWatt Technologies, Inc. Dr. Heydari is a Guest Editor of IEEE JOURNAL OF SOLID-STATE CIRCUITS. He currently serves on the Technical Program Committees of Compound Semiconductor IC Symposium (CSICS), and. He was an Associate Editor of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—I: REGULAR PAPERS from 2006 to 2008. He was a Technical Program Committee member of the IEEE Custom Integrated Circuits Conference (CICC), International Symposium on Low-Power Electronics and Design (ISLPED), IEEE Design and Test in Europe (DATE), and International Symposium on Quality Electronic Design (ISQED).