Energy Dissipation Modeling of Lossy Transmission Lines Driven by CMOS Inverters

Payam Heydari
Department of Electrical and Computer Engineering
University of California
Irvine, CA 92697

Abstract - *In this paper, new formulations for the energy dissipation of lossy transmission lines driven by CMOS inverters are provided. These formulations are obtained using an approximated expression for the driving-point impedance of lossy coupled transmission lines which itself is derived by solving Telegrapher's equations. A comprehensive analysis of energy is performed for both step and flattened ramp inverter inputs. To accomplish this task, a new stable circuit that is capable of modeling the transmission line for a broad range of frequencies is synthesized. Experimental results show that the energy calculated using this equivalent circuit is almost equal to the one calculated by solving the more complicated transmission line equations directly.*

1. Introduction

The semiconductor industry is continually moving toward the development and the implementation of smaller technology sizes, and as a result enabling a host of new and powerful applications. Recent studies on the effects caused by the nanometer technologies focus primarily on timing and signal integrity [1]. However, only a handful of works have actually considered the deep sub-micron (DSM) effects on the energy dissipation of ULSI circuits [2][3]. Global interconnects dissipate a large amount of energy that is supplied by the power-supply voltage to the circuit. The wiring system of a one-billion transistor die will deliver signal and power to each transistor on the chip, provide low-skew and low-jitter clock to latches, flip-flops and dynamic circuits, and also distribute data and control signals throughout the chip [4]. Providing the required global connectivity throughout the whole chip demands long on-chip wires. These global wires should deliver high frequency signals (presently at around 1.5-2.5GHz) to various circuits. This implies that the global wires exhibit transmission line effects. So far, the well-known $(1/2)CV^2$ model has been used as an interconnect energy model, where C includes the capacitance of the interconnect and the capacitances of the driven circuits, and V is the voltage swing. This model, however, fails to predict the interconnect energy dissipation in the current range of clock frequencies, where the signal transients do not usually settle to a steady state value due to the small clock periods. In paper [2], an analytical interconnect energy model with consideration of event coupling has been proposed. Although this work considers the crosstalk effect on the interconnect energy dissipation, it uses the distributed ladder RLC circuits to model the lossy transmission line effects. In paper [5], authors showed that using distributed RLC circuits do not capture all behaviors of lossy transmission lines that can be captured otherwise using the transmission line equations.

In this paper, accurate expressions for the energy dissipation of interconnects driven by CMOS inverters are obtained under two inverter inputs; a step input, and a flattened ramp input. The dissipated energy is derived using an approximated expression for the driving-point impedance of lossy transmission lines.

Section 2 presents a new RLC circuit configuration called RLC-π circuit, whose driving-point impedance can accurately estimate the driving-point impedance of lossy transmission line. In section 3, the RLC-π circuit is utilized to derive the total energy dissipation of a transmission line driven by a CMOS inverter. For the sake of completeness, the energy calculation is performed for both the step input and the flattened ramp input. Simulations and experimental results provided throughout this section confirms the accuracy of our model. Finally, section 4 presents the conclusions of our paper.

2. An accurate lower-frequency model for the lossy transmission line

In present-day digital and mixed-signal integrated circuits, the global on-chip interconnects must provide the required connectivity and performance for clock rates of 1.5-2.5GHz, which is in a microwave frequency range. This certainly demands a knowledge of electromagnetic-field theory to analyze the on-chip wiring effects. A related question that arises is whether the transmission line effects of on-chip interconnects can have any affect on the energy dissipation. This section addresses this question in details.

The critical global interconnections, such as clock lines, control lines, and data buses (which can be 32-128 bits wide) between processor and on-chip cache reach more than 100K connections. The propagation delay of signals traveling through these global wires is comparable to the time of flight. In other words, the line length is comparable to the propagated signal wavelength, λ, which is on the order of 0.7-2.2*cm*. This implies that transmission-line properties have to be taken into account. It was shown in [5] that any two uniform parallel conductors, the signal and the return paths, that are used to transmit electromagnetic energy can be considered transmission lines. The return path can be a ground plane, a ground conductor, or a mesh of ground lines on many layers. Solutions to Maxwell's equations for the electric and magnetic fields around conductors are current and voltage waves. The solution is completely determined in terms of the *characteristic impedance*, Z_o, and the *propagation constant*, γ. Consider a single transmission line as shown in Fig. 1.

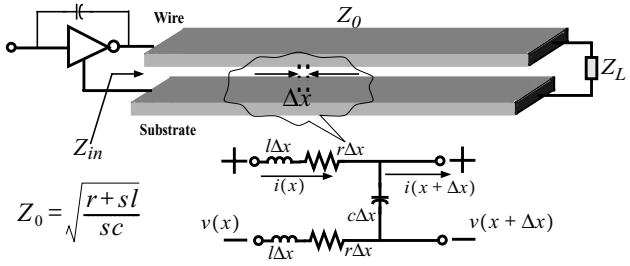

Fig. 1. The schematic of a lossy transmission line along with the circuit representation of a differential length Δx

The driving-point impedance of this transmission line is obtained using the voltage and current wave equations at the input port:

$$Z_{in}\big|_{x=-h} = \frac{V_i e^{\gamma h} + V_r e^{-\gamma h}}{I_i e^{\gamma h} - I_r e^{-\gamma h}} = Z_0\left(\frac{1+\Gamma_L e^{-2\gamma h}}{1-\Gamma_L e^{-2\gamma h}}\right) = Z_0\frac{Z_L + Z_0\tanh(\gamma h)}{Z_0 + Z_L\tanh(\gamma h)} \quad (1)$$

where h is the line length. In the above equation, the load impedance, Z_L, is normally a capacitive load in ULSI circuits, since the interconnect normally drives a CMOS circuit whose input impedance is purely capacitive.

According to Eq. (1), the input impedance of a transmission line is a nonlinear function of frequency. Direct substitution of this nonlinear expression into the energy equation (which is the integral of the voltage-current product) does not yield a closed-form expression for the energy dissipation of the lossy transmission line. Still it is possible to simplify Eq. (1), using some observations, and obtain an accurate expression for the energy dissipation. *If the abrupt transitions of the input waveform are sufficiently far away in time so as to allow the circuit to come very close to its steady-state response, then the total energy delivered by the input source is obtained using the driving point impedance evaluated at low frequencies*. This observation is utilized here to simplify Eq. (1). As a first step, we evaluate *tanh*(.) at low frequencies:

$$\tanh(\gamma h) = \frac{\sinh(\gamma h)}{\cosh(\gamma h)} \rightarrow \frac{2\gamma h}{2+\gamma^2 h^2} \quad , \textit{ for small values of } |s| \quad (2)$$

This leads to the following relationship:

$$Z_{in}\big|_{x=-h} = \frac{1}{C_L s}\left[\frac{2+\gamma^2h^2+\left(2\gamma^2h^2\ \frac{C_L}{C_{int,tot}}\right)}{2+\gamma^2h^2\ \ +\left(2\ \frac{C_{int,tot}}{C_L}\right)}\right] \quad (3)$$

where $C_{int,tot}$ is the interconnect capacitance including the Miller capacitance of the neighboring lines that are capacitively coupled to this line, and the interconnect-to-substrate capacitance.

It would be instructive if one could propose a stable circuit realization whose impedance is expressed by Eq. (3) which is actually a rational transfer function. For a lossy transmission line whose driving-point impedance near the DC frequency is expressed by Eq. (3), a new stable RLC-π equivalent circuit realization can be synthesized as demonstrated in Fig. 2. $L_{int,tot}$ is the total inductance of the lossy line including the self and mutual inductances. The inductive couplings between transmission lines are accounted for by an algebraic summation of each line's self inductance and all mutual inductances between that line and other lines considering also the current direction flowing through the lines. For example in a set of N coupled transmission lines, the total per unit length inductance of the *j*-th line that is magnetically coupled to other lines is:

$$l_{int,tot\ j} = \ l_{int\ j} + \sum_{i \neq j}(\pm M_{ij})$$

R_{int} is the line resistance. C_1, C_2, and C_3 are related to actual capacitances of the line and the load through the following relationships:

$$C_3 = \sqrt{\frac{(C_{int,tot}+C_L)^2+C_L^2}{2}},\ C_2 = \frac{C_{int,tot}}{2}+C_L-C_3,\ C_1 = C_{int,tot}+C_L-C_3 \quad (4)$$

The input impedance of the transmission line in Fig. 2 at lower-frequency ranges is:

$$Z_{in,xline}(s) = \left(\frac{1+2C_L/C_{int,tot}}{C_L s}\right)\left(\frac{s^2+\frac{R_{int}}{L_{int,tot}}s+\frac{2}{L_{int,tot}C_{int,tot}(1+2C_L/C_{int,tot})}}{s^2+\frac{R_{int}}{L_{int,tot}}s+\frac{2(1+C_{int,tot}/C_L)}{L_{int,tot}\ C_{int,tot}}}\right) \quad (5)$$

The input impedance of the RLC-π circuit depicted in Fig. 2 is:

$$Z_{in,\,RLC}(s) = \frac{1}{(C_1+C_2 \circledS C_3)s}\left(\frac{s^2+\frac{R_{int}}{L_{int,tot}}s+\frac{1}{L_{int,tot}(C_2+C_3)}}{s^2+\frac{R_{int}}{L_{int,tot}}s+\frac{(C_1+C_3)/(C_2+C_3)}{L_{int,tot}(C_1+C_2 \circledS C_3}}\right) \quad (6)$$

where $C_2 \circledS C_3$ represents the series combination of C_2 and C_3. Equating the *s* coefficients of the driving-point impedance $Z_{in,xline}(s)$ of the transmission line with those of the input impedance $Z_{in,\,RLC}(s)$ of the proposed RLC circuit verifies the circuit equivalence.

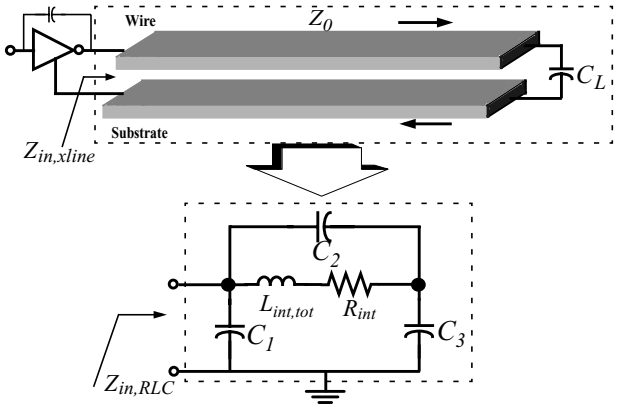

Fig. 2. A lossy transmission line and its equivalent RLC-π circuit representation

Fig. 3 shows the magnitude response of the driving-point admittance of a lossy transmission line which is electromagnetically coupled to a similar line. First, the circuit is simulated using star-HSPICE. Eq. (1) is then utilized and the magnitude response of the admittance function (which is the inverse of the impedance function) is calculated. As indicated in Fig. 3, the results obtained by HSPICE and by Eq. (1) are exactly the same and are indistinguishable from each other. In the next step, Eq. (6) is utilized to calculate the magnitude response of the driving-point admittance for the equivalent RLC-π circuit. According to Fig. 3, this circuit accurately represents the driving-point admittance of a lossy coupled transmission line in lower frequencies up to 670MHz (2Grad/sec). Consequently, the energy calculations using the RLC-π circuit yield expressions that are exactly equal to those of the actual coupled lossy line.

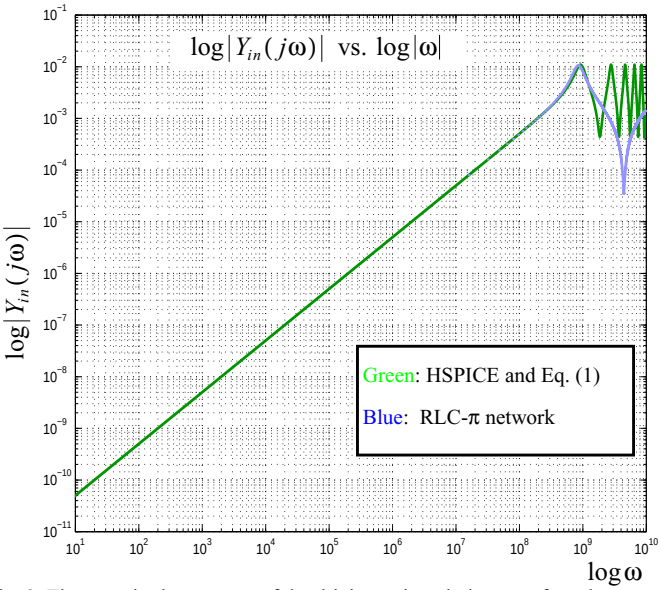

Fig. 3. The magnitude response of the driving point admittance of an electromagnetically coupled lossy transmission line obtained using HSPICE simulation, using the direct simulation of Eq. (1), and by replacing the line with its equivalent RLC-π circuit

The RLC-π equivalent circuit synthesized for a lossy coupled transmission line is used to compute the driving point impedance and interconnect energy calculation. The effect of the input source impedance on the total energy dissipation is readily taken into account by connecting the input terminal of the equivalent RLC-π to input source. Using the equivalent RLC-π circuit, section 3 provides a comprehensive analysis of energy dissipation in the lossy transmission lines driven by CMOS inverters.

3. Energy Dissipation of Lossy Transmission Lines

Consider the circuit shown in Fig. 2. that is composed of an inverter driving a lossy transmission line. The load is another CMOS gate that is connected to the other port of this lossy transmission line. The electromagnetic coupling effects are treated the same way as we discussed in section 2. Fig. 4. shows the equivalent RLC-π circuit driven by a CMOS inverter that needs to be analyzed. The π structure of the RLC-π circuit makes the impedance calculations very simple. For instance, the diffusion and miller-effect capacitances of the driving CMOS circuits (C_d in Fig. 4) are placed directly in parallel with the capacitance, C_1 of the RLC-π circuitry and consequently no additional calculation is required.

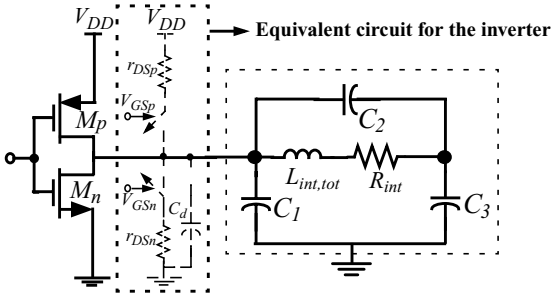

Fig. 4. The equivalent RLC-π circuit model of a lossy coupled transmission line driven by a CMOS inverter

Due to the changes in the operation regions of NMOS and PMOS transistors of the inverter during low-to-high and high-to-low transitions of the inverter's output, we must distinguish between low-to-high and high-to-low transitions. During the low-to-high transition at the output,

the PMOS transistor is conducting and provides a low-impedance conduction path from the supply to the load. During the high-to-low transition at the output the NMOS transistor is in "ON" condition, and no additional energy is transferred out of the power-supply.

We calculate the energy transferred out of the power-supply during a low-to-high transition. This energy is the total dissipated energy per clock period of a CMOS gate that drives another CMOS circuit through a coupled lossy transmission line. The energy delivered by the power-supply through the gate in a low-to-high transition of the output is specified by Eq. (7).

$$E_{tot} = \int_{(L \to H)} V_{DD}\, i_{DD}(t)\, dt \tag{7}$$

where $i_{DD}(t)$ is the current flowing from the power-supply to the output and through the PMOS transistor during the low-to-high transition of the output. The interconnect energy analysis is done thoroughly for two common input waveforms: a step input, and a flattened ramp input.

3.1. Energy calculation for a step input

Consider the circuit shown in Fig. 4, where the input to the inverter is a step function $v_{in}(t) = V_{DD}u(t)$) ($u(t)$ is the unit step function). Although in reality all voltages and currents have finite slew times, addressing the step response provides a good intuition about the transient and steady-state response of the circuit under the realistic inputs. We calculate the energy transferred out of the power-supply during a low-to-high transition. The current is obtained using the driving point admittance of the circuit indicated by Fig. 4:

$$I_{DD}(s) = \frac{V_{DD}}{s} Y_i(s)$$

where $Y_i(s)$ is the driving-point admittance seen from the power-supply to the source connection of the PMOS transistor in Fig. 4. $Y_i(s)$ is the parallel combination of $Y_{in,RLC}(s) = 1/Z_{in,RLC}(s)$, the equivalent capacitance of the driving inverter, C_d. This equivalent capacitance is a parallel combination of the diffusion capacitance C_{diff} of MOS devices, and the miller-effect of the gate-drain capacitances; $2(C_{GDp}+C_{GDn})$. We distinguish between the overdamped and the underdamped responses. The energy delivered by the supply voltage will be derived for each of these responses in the next two subsections.

3.1.1. Underdamped response

In the underdamped case, the voltage and current transient waveforms oscillate toward their steady-state values. If $R_{int} < 2\sqrt{L_{int,tot}/(C_2+C_3)}$ then the current and voltage waveforms will oscillate until they reach their steady state value. To obtain the total energy transferred out of the power supply Eq. (7) is used. The input current to the circuit is first obtained by solving the characteristic differential equation of the RLC-π circuit:

$$i_{DD} = (C_d + C_{eq,\pi})V_{DD}\delta(t) + \frac{V_{DD}}{L_{int,tot}\omega_{d,\pi}} \left(\frac{C_3}{C_2+C_3}\right)^2 e^{-\alpha_\pi t}\sin\omega_{d,\pi}t \tag{8}$$

where $C_{eq,\pi} = C_1 + C_2 \textcircled{\$} C_3$ is the equivalent capacitance of the RLC-π circuit, $\alpha_\pi = R_{int}/2L_{int}$, $\omega_{p,\pi}^2 = 1/(L_{int}(C_2+C_3))$, and $\omega_{d,\pi} = \sqrt{\omega_{p,\pi}^2 - \alpha_\pi^2}$. C_1, C_2, and C_3 are given by Eq. (4). The total energy delivered by the power-supply is:

$$E_{u,step}^{xline} = (C_d + C_1 + C_3)V_{DD}^2 - \left(\frac{C_3^2}{C_2+C_3}\right)V_{DD}^2 \left(\frac{\omega_{p,\pi}}{\omega_{d,\pi}}\right) e^{-\frac{\alpha_\pi T}{2}} \sin\left(\frac{\omega_{d,\pi}T}{2} + \Phi_\pi\right) \tag{9}$$

Remember that $C_1 + C_3 = C_L + C_{int,tot}$. It is observed that if a CMOS inverter driving a lossy coupled line undergoes an underdamped oscillatory response, and if $R_{int}/L_{int,tot} >> 4\pi f_{clock}$ (or if $1/(2\pi\sqrt{L_{int,tot}(C_2+C_3)}) >> 2f_{clock}$), then the energy expression becomes:

$$E_{u,step}^{xline} = (C_d + C_{int,tot} + C_L)\ V_{DD}^2 \tag{10}$$

Equations (9) and (10) give the actual and steady-state energy dissipation per clock period, respectively, when the circuit experiences an underdamped oscillatory transient response.

3.1.2. Overdamped response

In the overdamped case, the resistance, R_{int} is sufficiently large (i.e., $R_{int} > 2\sqrt{L_{int,tot}/(C_2+C_3)}$) such that it eliminates the resonances from current and voltage waveforms. Once again, to obtain the total energy transferred out of the power supply using Eq. (7), the input current to the circuit is first obtained by solving the characteristic differential equation of the RLC-π circuit:

$$i_{DD} = (C_d + C_{eq,\pi})V_{DD}\delta(t) + \frac{V_{DD}}{L_{int,tot}\alpha_{d,\pi}} \left(\frac{C_3}{C_2+C_3}\right)^2 e^{-\alpha_\pi t}\sinh\alpha_{d,\pi}t \tag{11}$$

where $\alpha_{d,\pi} = \sqrt{\alpha_\pi^2 - \omega_{p,\pi}^2}$. The total energy delivered by the power-supply for the overdamped transient response is:

$$E_{o,step}^{xline} = (C_d + C_1 + C_3)V_{DD}^2 - \left(\frac{C_3^2}{C_2+C_3}\right)V_{DD}^2 \left(\frac{\omega_{p,\pi}}{\alpha_{d,\pi}}\right) e^{-\frac{\alpha_\pi T}{2}} \sinh\left(\frac{\alpha_{d,\pi}T}{2} + \Psi_\pi\right) \tag{12}$$

It turns out that if a CMOS inverter driving a lossy coupled line has an overdamped response, and if $\alpha_\pi - \alpha_{d,\pi} >> 4\pi f_{clock}$, then the energy dissipation per each clock period becomes:

$$E_{o,step}^{xline} = (C_d + C_{int,tot} + C_L)\ V_{DD}^2 \tag{13}$$

Equations (12) and (13) give the actual and the steady-state energy dissipation per clock period, respectively, when the circuit experiences an overdamped transient response.

3.2. Energy calculation for a flattened ramp input

Let us consider the circuit shown in Fig. 4 under a flattened ramp input $v_{in}(t) = (V_{DD}/t_r)[tu(t) - (t-t_r)u(t-t_r)]$. In this case, the operating regions of the conducting transistors change during the input transition. This change in the operating regions of the transistors makes the analysis cumbersome. To simplify the formulations, two important observations are taken into account. First of all, in deep submicron regime short channel effects including velocity saturation can have a drastic influence on I_D-V_{DS} characteristics of a MOS transistor. Most notably, the saturation is achieved at smaller values of V_{DS}. Secondly, for the fast input ramp, the conducting transistors operate in the linear region for a large portion of the time [6]. As a result, we assume that a conducting transistor will be in the linear region for the entire input transition.

Once again the energy transferred out of the power supply during a low-to-high transition is calculated. The driving current of the RLC-π circuit under a flattened ramp input is:

$$I_{DD}(s) = \frac{V_{DD}}{t_r s^2}(1 - e^{-t_r s})\, Y_i(s) \tag{14}$$

Similar to the step input, we distinguish between the overdamped and underdamped outputs and for each output response derive the energy.

3.2.1 Underdamped response

Similar to the step input case, if $R_{int} < 2\sqrt{L_{int,tot}/(C_2+C_3)}$ then current and voltage will experience a damped oscillatory waveform. To calculate the current expression, the input is expressed as an algebraic summation of two ramp inputs, where the one of the ramp waveforms is a delayed version of another one. The circuit response is obtained for one input ramp. The response to the delayed ramp input is obviously the delayed version response to the first ramp. Omitting the details of mathematical calculations, the output current response is as follows:

$$i_{DD} = i_D(t) - i_D(t-t_r) \tag{15}$$

where:

$$i_D = (C_d + C_1 + C_3)\frac{V_{DD}}{t_r}\left[1 - \frac{C_3 - C_3 \textcircled{\$} C_2}{C_d + C_1 + C_3}\left(\frac{\omega_{p,\pi}}{\omega_{d,\pi}}\right) e^{-\alpha_\pi t}\sin(\omega_{d,\pi}t + \Phi_\pi)\right]u(t) \tag{16}$$

In the energy expression given by Eq. (7), the current i_{DD} is substituted by equations (15) and (16). The total energy transferred out of supply voltage is thus equal to:

$$E_{u,ramp}^{xline} = (C_d + C_1 + C_3)\ V_{DD}^2 - \left[E_{osc}\left(\frac{T}{2}\right) - E_{osc}\left(\frac{T}{2} - t_r\right)\right] \tag{17}$$

where

$$E_{osc}\left(\frac{T}{2}\right) = \frac{V_{DD}^2}{t_r}\left(\frac{C_3 - C_3 \textcircled{\$} C_2}{C_1 + C_3 \textcircled{\$} C_2}\right)\frac{1}{\omega_{d,\pi}} e^{-\frac{\alpha_\pi T}{2}} \sin\left(\frac{\omega_{d,\pi}T}{2} + 2\Phi_\pi\right) \tag{18}$$

Here it can be easily verified that if the natural resonant frequency of the RLC-π equivalent circuit is larger than the clock frequency, then the voltage and current waveforms reach their steady-state values and Eq. (17) becomes:

$$E_{u,ramp}^{xline} = (C_d + C_{int,tot'} + C_L)V_{DD}^2 \tag{19}$$

3.2.2 Overdamped response

Similar to the step input case, if the interconnect resistance is sufficiently high so that $R_{int} > 2\sqrt{L_{int,tot}/(C_2+C_3)}$, the current and voltage waveforms will be in the form of decaying exponential waveforms under a flattened ramp waveform at the inverter input.

Once again, the current waveform is an algebraic summation of two ramp inputs, where one of the ramp waveforms is a delayed version of another one:

$$i_{DD} = i_D(t) - i_D(t - t_r) \tag{20}$$

where

$$i_D = (C_d + C_1 + C_3)\frac{V_{DD}}{t_r}\left[1 - \frac{C_3 - C_3 \circledS C_2}{C_d + C_1 + C_3}\left(\frac{\omega_{p,\pi}}{\alpha_{d,\pi}}\right)e^{-\alpha_\pi t}\sinh(\alpha_{d,\pi}t + \Psi_\pi)\right]u(t) \tag{21}$$

The total energy transferred out of supply voltage is thus equal to:

$$E_{o,\,ramp}^{xline} = (C_d + C_1 + C_3)V_{DD}^2 - \left[E_{exp}\left(\frac{T}{2}\right) - E_{exp}\left(\frac{T}{2} - t_r\right)\right]$$

where

$$E_{exp}\left(\frac{T}{2}\right) = \frac{V_{DD}^2}{t_r}\left(\frac{C_3 - C_3 \circledS C_2}{C_1 + C_3 \circledS C_2}\right)\frac{1}{\alpha_{d,\pi}}e^{-\frac{\alpha_\pi T}{2}}\sinh\left(\frac{\alpha_{d,\pi}T}{2} + 2\Psi_\pi\right)$$

If a CMOS inverter driving a lossy coupled line has an overdamped response, and if $\alpha_\pi - \alpha_{d,\pi} >> 4\pi f_{clock}$, then the energy dissipation per each clock period becomes:

$$E_{o,\,ramp}^{xline} = (C_d + C_{int,tot} + C_L)\,V_{DD}^2 \tag{22}$$

In the energy calculations of interconnects driven by CMOS circuits, it was normally assumed that transients in the current and voltage waveforms have been settled to steady state values and the energy was thus simply equal to $(1/2)CV_m^2$. We showed that this expression can yield quite an inaccurate result for the dissipated energy of the interconnect in high frequency ULSI circuits. Figures 5 and 6 show that modeling a lossy transmission line with a single RLC circuit do not still provide accurate results for the dissipated energy in both underdamped and overdamped cases. These figures show the dissipated energy of a single lossy transmission line for various line lengths when the line is modeled by the RLC-π circuit and compare it with that obtained using a single RLC circuit. For small clock cycles, the RLC circuit model is unable to give a good energy estimate. This is true for both overdamped and underdamped circuits. Figures 5 and 6 also reveal that for both underdamped and overdamped circuits when the clock cycle time is sufficiently long, the results obtained by energy calculations in RLC and RLC-π circuits are both closely equal to $(1/2)CV_m^2$.

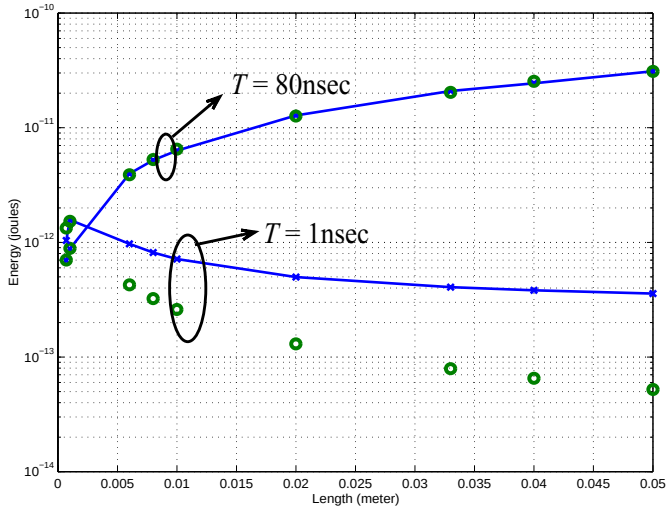

Fig. 5. A comparison between the energy-length variation of the equivalent underdamped RLC-π circuit and that of single underdamped RLC circuit of a lossy transmission line. The comparison has been made for two values of cycle time, T = 1nsec and T = 80nsec

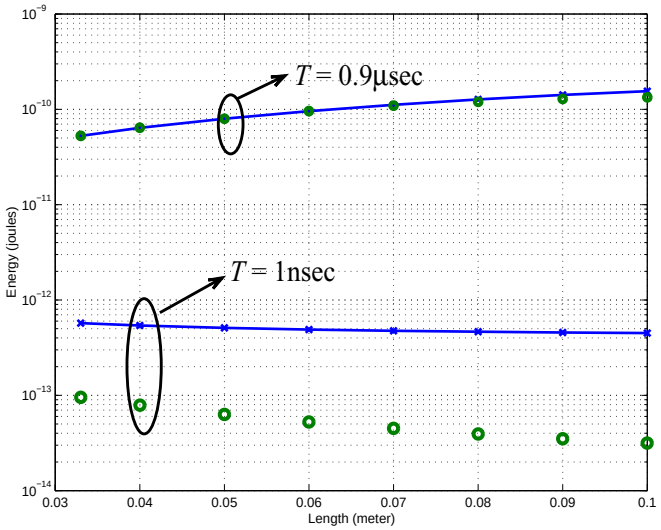

Fig. 6. A comparison between the energy-length variation of the equivalent overdamped RLC-π circuit and that of single overdamped RLC circuit modeling a lossy transmission line. The comparison has been made for two values of cycle time, T = 1nsec and T = 0.9μsec

4. CONCLUSION

This paper presented accurate closed-form expressions for the interconnect energy dissipation in high-speed ULSI circuits. The energy was calculated using an approximate expression for the driving-point impedance of a lossy transmission line. We synthesize a new stable circuit that is capable of modeling the transmission line for a broad range of frequencies. A comprehensive analysis was incorporated to derive the dissipated energy of a lossy transmission line under the two different inputs; a step input, and ramp input. Several experimental results show that the energy calculated using this circuit is almost equal to the one calculated by directly solving the complicated transmission line equations.

Acknowledgement

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