Experimental Analysis of Biasing Voltage Generation in Wave-Controlled RIS

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***Abstract*—Reconfigurable intelligent surfaces (RISs), an emerging technology proposed for inclusion in next-generation wireless communication systems, are programmable surfaces that can adaptively reflect/scatter incident electromagnetic radiation in different desired directions. To reduce the complexity and physical profile of conventional RIS designs, a novel concept known as Wave-Controlled RIS has been proposed, in which standing waves along a transmission line are used to generate the required dc bias for reflective control. This paper presents a proof-of-concept design and experimental characterization of a biasing transmission line (BTL) to control a Wave-Controlled RIS. As important design considerations, the effects of generator-BTL impedance mismatch, distributed rectifier loading, and nonideal peak detection are quantified using a transmission-line model, nonlinear circuit-electromagnetic co-simulations, and measurements. Additionally, the potential for reflective control using only a single standing wave frequency on the biasing transmission line is explored, demonstrating the ability of single-beam steering toward angles near broadside, while identifying practical limitations and opportunities for optimizing the BTL, rectifier, and RIS unit cell.**

***Index Terms*—beamforming, biasing transmission line (BTL), reconfigurable intelligent surface (RIS), standing waves, varactor-based tuning, wave-controlled bias generation.**

I. Introduction

THE implementation of reconfigurable intelligent surface (RIS) technology presents a novel way to improve wireless communication performance by providing adaptive degrees of freedom to design radio-frequency (RF) channels. Using an RIS, signals can be steered around obstacles, beamforming gains can be increased to boost signal-to-noise ratio (SNR) and lower interference, and the overall quality of service (QoS) experienced by network users can be greatly enhanced [1]. RIS technology is especially beneficial in challenging RF environments like urban areas and indoor spaces, where it can be difficult to sustain strong and reliable signal transmissions [2].

An RIS consists of a large number of reconfigurable sub-wavelength components, such as metallic patches, that are electronically controlled to manipulate electromagnetic waves [3]. These unit cells have the ability to precisely control how incoming electromagnetic waves behave by dynamically modifying their reflection characteristics in real time using tunable elements such as PIN diodes, varactor diodes, and liquid crystals, among others [4]. RISs can increase signal strength, boost wireless network performance, and open the door for more effective communication systems by optimizing wave reflection and propagation.

RIS designs can have hundreds to thousands of unit cells operating at millimeter-wave and terahertz frequencies, resulting in notable beamforming gains and allowing for highly directed and reconfigurable beams [5], [6]. Although these qualities improve communication, there are several obstacles to overcome when implementing large-scale RIS designs. Most RIS systems depend on external control units, such as field-programmable gate arrays (FPGAs) or microcontrollers, to configure the reconfigurable elements on the RIS surface [7]. For an RIS with M elements, these control units perform optimization processes involving M variables and transmit the optimal configuration to each of the M RIS elements. Thus, each unit cell requires a dedicated connection to receive the appropriate control voltages or currents, leading to complex wiring networks with hundreds of individual signal connections. This not only complicates fabrication but also increases hardware costs and limits practical deployment. Alternative control strategies such as light-based approaches employing photodiodes, scanning lasers, or encoded light images have been investigated in order to overcome these difficulties [8]–[12]. Despite their potential, these methods face limitations, including susceptibility to environmental factors such as rain and reduced resolution due to the distance between the light source and the RIS.

This paper investigates the performance of the technique presented in [13] and later studied in [14]–[19] as a realistic and effective way to control RIS elements. Unlike earlier treatments, this work validates a complete biasing chain driven by a single biasing standing wave (BSW) through impedance analysis, circuit–electromagnetic co-simulation, and experimental characterization of rectifier loading and temporal response. It also provides a more comprehensive analysis of single-BSW reflection control, addressing specular nulling, the effects of short- and open-circuit BTL terminations and array length, and the near-broadside steering conditions; and further derives an analytical relationship between the BSW frequency and the target steering angle. A schematic is shown in Fig. 1. This technique, utilizing varactors for reconfigurable reflective control, consists of delivering dc biasing voltages to the varactors inside the unit cells that are connected at specific positions, x_m, along a single biasing transmission line (BTL). The desired dc biasing voltages supplied to every

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RIS element to achieve a specific reflective radiation pattern, $w(m)$, can be obtained from combinations of N BSWs, $w(x_m, t)$, that are injected into the BTL. The scope of this paper is limited to the study of the performance of the BTL when only a single frequency is used. Further, the extent to which a single reflected beam can be controlled through this single biasing frequency is explored. The prototype is intended as a proof of concept rather than a fully optimized RIS implementation. In particular, the selected peak-detector topology, the BTL geometry and matching, and the tunable RIS unit cell constitute one practical realization and can be optimized for lower loading, smaller ripple, faster response, and a wider reflection-phase range. This technique drastically lowers signaling overhead and hardware complexity by doing away with the requirement for separate wired connections to every unit cell. Advanced RIS functions, including beam creation, polarization control, and channel equalization, are made possible by this straightforward yet efficient control method, which makes it a viable option for large-scale RIS deployments.

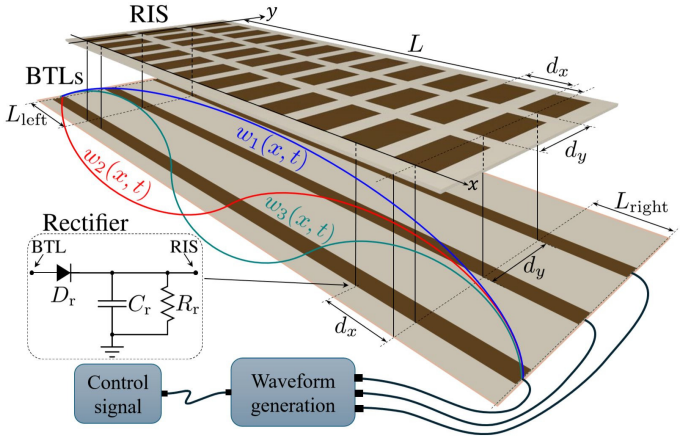


Fig. 1: Wave-Controlled RIS System: The top layer consists of M RIS elements along the x direction in each row, which are metallic patches connected to varactors uniformly spaced by d_x. The bottom layer contains N biasing standing waves $w_n(x,t)$ that are excited on each BTL. Rectifiers uniformly spaced by d_x in the x direction are used to generate the dc biasing voltages for the varactors. Each BTL is controlled through only one connection on the right, where the N frequencies are injected. Here, a straight-line BTL is shown for conceptualization, although in our experiments we use a meandered line to achieve very low-frequency BSWs.

II. Biasing Standing Waves

To use a wave-controlled feed network for the RIS, an analytical model for the voltages was derived from a transmission line analysis of the system. This model determines the control voltages that are applied to the unit cells by the input wave, and thus is necessary for understanding how the unit cells are reconfigured.

The wave-controlled RIS approach involves two key components: a BTL board and an RIS board, as shown in Fig. 1. The BTL board, placed beneath the reflective surface and shielded from RF interference by a ground plane, supports N BSWs. Rectifiers placed at M positions on the BTL board generate dc voltages, $w(m)$, from these waves, which are used to bias the M varactors positioned on the RIS board at x_m for $m = 0, 1, \ldots, M-1$. This process modifies the reflected phase distribution, enabling control of the RIS's scattered radiation pattern [16]. The voltage applied to each varactor, $w(m)$, for a given reflected phase is calculated using an analytical model for the varactors that accounts for the RIS's reflection behavior under various dc bias conditions [16], [20]. Once the required voltages are determined, they are generated by a periodic time-domain signal comprising a combination of N BSWs with specified amplitudes W_n, for $n = 1, 2, \ldots, N$, that are injected into the BTL through a single input port, along with a base voltage W_0. The inclusion of W_0 simplifies reconstruction of the voltage distribution, as the varactor's biasing voltage range typically does not include 0 V. Consequently, the expected voltage distribution pattern includes a dc component.

As seen on the RIS board in Fig. 1, the RIS unit cells are separated by a distance d_x along the x direction. Likewise, the corresponding rectifiers that convert the standing wave amplitudes, $w_n(x_m, t)$, into dc values for each RIS unit cell are also separated by a distance d_x in the x direction along the BTL board. These, along with the voltage offset W_0, produce the necessary voltages $w(m)$ [16]. The position along the BTL of the mth rectifier element is consequently defined as $x_m = md_x$. The BTL board is not necessarily as simple as that shown in Fig. 1, an example of which is provided in [15]. This BTL must connect with the RIS board at specific positions along the x direction within the length L, where $L = (M-1)d_x$. The total length of the BTL in the x direction is thus defined as $L_{\text{tot}} = L + L_{\text{left}} + L_{\text{right}}$, where L_{left} and L_{right} are additional segments on either end of the BTL that help refine the voltage distribution pattern across the M elements. The phase velocity of the propagated modes projected along the x direction is $v_{\text{b}} = c/n_{\text{slow}}$, where c represents the speed of light and $n_{\text{slow}} \geq 1$ is a slowness factor determined by the effective permittivity of the substrate and geometry of the BTL (a meandered microstrip line, in the present case). The injected periodic time-domain signal oscillates at the biasing frequency $f_{\text{b}} = v_{\text{b}}/\lambda_{\text{b}}$, where $\lambda_{\text{b}} = 2\pi/k_{\text{b}}$ is the guided wavelength, and the corresponding propagation wavenumber is $k_{\text{b}} = 2\pi f_{\text{b}}/v_{\text{b}}$.

The slowness factor, n_{slow}, is an important BTL design parameter, since it sets f_{b} to establish the desired BSW pattern and the spacing between its harmonics. In particular, increasing the electrical path length of the meandered BTL relative to the physical distance between adjacent RIS elements reduces the phase velocity of the biasing waves, thereby increasing n_{slow}. This enables the use of lower BSW frequencies, which is also advantageous because it increases the spectral separation between the biasing harmonics and the RF operating band of the RIS. However, increasing n_{slow} also introduces practical trade-offs. Larger slowness factors require longer and more compact meandered paths, which can increase ohmic and dielectric losses along the BTL and make the standing waves more sensitive to attenuation and fabrication tolerances. In addition, the usable harmonic range is also limited by BTL attenuation and mismatch. Thus, n_{slow} must balance harmonic availability, losses, and spectral separation from the RF band.

This design approach enables modeling of the BSW voltage before and after each rectifier. The voltage of the standing wave at any point along the BTL can be derived by applying

transmission line theory [21]. In the general case, when there are N biasing modes (degrees of freedom to control the RIS response), the biasing voltage of the standing wave before rectification, assuming a short-circuit termination at $x = -L_{\text{left}}$, is [13], [16], [18]

$$w(x,t) = W_0 + \sum_{n=1}^{N} W_n \sin\left(\frac{n\omega_\text{b} n_\text{slow}}{c}\left(x + L_\text{left}\right)\right)\cos\left(n\omega_\text{b} t + \phi_n\right). \tag{1}$$

Here, n is the biasing mode index and W_n is the real-valued amplitude of the standing wave of the nth biasing mode. The term W_0 is the dc component, which sets the minimum biasing voltage applied to the BTL and shifts the varactor's operating range. Furthermore, ϕ_n is the phase offset of the nth biasing mode. This definition generalizes Eq. (7) of Ref. [16], as here the wavelength λ_b and, consequently, the fundamental frequency f_b, do not necessarily depend on the total length of the BTL L_tot; in other words, we do not need standing waves that are resonant with the BTL length.

The mth rectifier, shown in Fig. 1, acts as a peak detector and is described in detail in Sec. III. Its ideal output voltage is given by

$$w(m) = W_0 + \max_t \left[\sum_{n=1}^{N} W_n \sin\left(\frac{n\omega_\text{b} n_\text{slow}}{c}\left(x_m + L_\text{left}\right)\right)\cos(n\omega_\text{b} t + \phi_n)\right]. \tag{2}$$

This description neglects BTL losses, geometry and coupling, and distributed rectifier loading and losses. Their effects are discussed in Sec. IV-C and Appendix B. In [13], [16], we have explored theoretically the use of the BTL with several standing waves. Here, we focus on the experimental characterization of a BTL and on the use of a single BSW to control the pointing angle of a single beam. Accordingly, when using a single BSW of frequency f_b, (1) reduces to

$$w(x,t) = W_0 + W_\text{b} \sin\left(\frac{\omega_\text{b} n_\text{slow}}{c}\left(x + L_\text{left}\right)\right)\cos\left(\omega_\text{b} t + \phi\right), \tag{3}$$

where W_b is the amplitude and ϕ is the phase shift. After rectification at each x_m, the dc voltage is

$$w(m) = W_0 + \left|W_\text{b} \sin\left(\frac{\omega_\text{b} n_\text{slow}}{c}\left(x_m + L_\text{left}\right)\right)\right|. \tag{4}$$

III. System Design

The wave-controlled RIS is realized here using two separate boards: the RIS board and the BTL board. The RIS board reflects the incident radiation based on a spatial distribution of the RIS phase reflection coefficients, which is governed by the biasing voltage distribution $w(m)$ provided by the BSW, supported by the BTL board. Other implementations could be realized in a single multilayer board. This biasing pattern is controlled by the signal frequencies and amplitudes injected into the BTL (see Fig. 1). The RIS unit cell is designed to achieve the desired phase response by applying a variable voltage to the varactor. The design includes the unit-cell geometry, materials, and varactor. The BTL board comprises a transmission line with a defined geometry and integrated rectifiers to provide the dc biasing voltage for the unit cells of the RIS. Material specifications play a crucial role in the overall performance of the BTL and are introduced next.

A. RIS Unit Cell Design

The RIS unit cell consists of an array of two rectangular patches arranged in a mirrored configuration as shown in Fig. 2, mounted on a grounded dielectric substrate (RT5880LZ) with a relative permittivity of $\epsilon_r = 2$, a loss tangent of $\tan\delta = 0.0021$, and a thickness of 1.27 mm. Each patch is connected to the cathode of an individual SMV1231-040LF varactor, while the varactor's anode is grounded via a through-hole connection. We assume an incident y-polarized electric field, and the unit cell design is optimized to maximize the phase dynamic range within the industrial, scientific, and medical (ISM) 2.45 GHz band for reverse bias voltages ranging from 4 V to approximately 10 V.

The rectified reverse voltage $w(m)$ is provided to a varactor on the top RIS layer in the mth unit cell through a vertical biasing via from the center of the RIS patch to a coplanar waveguide on the ground plane of the RIS board (Fig. 2). This line is oriented to avoid disrupting the RIS ground-plane current, allowing efficient biasing of the varactors while minimizing the effect on the RIS RF current flow. To further suppress the effect on the RF current at the connection node located at the center of the coplanar waveguide, the capacitor $C_{r1} = 100$ pF is incorporated to ensure proper grounding at RF (Fig. 2). This capacitor is also part of the rectifier in the BTL board, as discussed in Sec. III B. The RIS board comprises 27 identical unit cells with two copper patches, with each unit cell featuring the following dimensions (in mm): $d_x = 20$, $A_1 = 18.5$, $A_2 = 1$, $A_3 = 0.3$, $B = 145.4$, $B_1 = 36.7$, $B_2 = 1.2$, $B_3 = 24.8$, $G_1 = 0.4$, $G_2 = 0.5$, $G_3 = 1.8$, $r = 0.2$, $P_1 = 4$, $P_2 = 0.4$, as shown in Fig. 2.

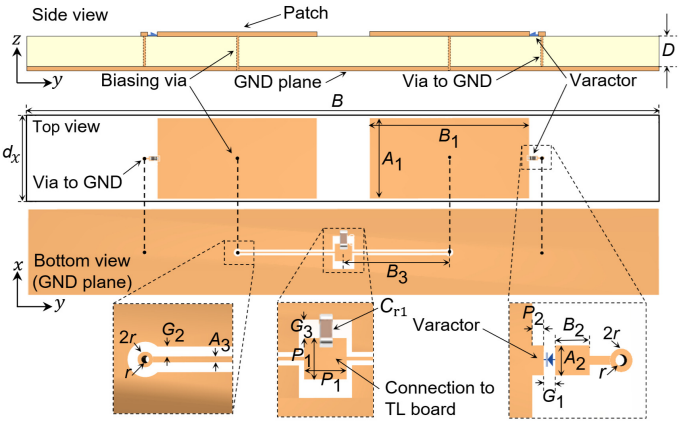


Fig. 2: RIS board unit cell. Two rectangular patches are arranged in a mirrored configuration on a grounded dielectric substrate. Each patch is connected to the cathode of an individual varactor with the varactor's anode grounded via a through-hole connection. The varactors are biased using a dc voltage provided by a via between the center of each patch and a coplanar waveguide with ground that is itself connected to the BTL board (not shown here).

To calculate the reflected phase provided by each RIS element, the analytical circuit model shown in Fig. 3 is

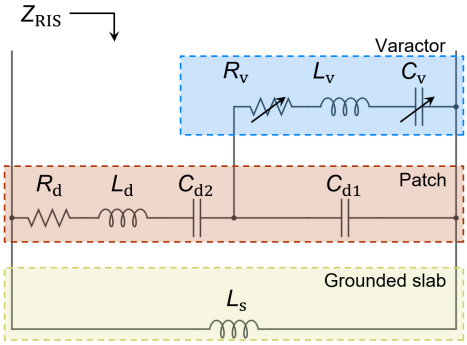


Fig. 3: Analytic circuit model to calculate the RIS impedance, Z_{RIS}, seen from a plane wave impinging from the top. Since this model accounts for the effect of the tunable varactor, the impedance Z_{RIS} is a function of the biasing voltage V.

summarized in [16], [18], [20]. This model requires only one full-wave simulation of the unit cell over the frequency of operation (assuming the varactor is disconnected) to extract the circuit elements that represent just the patch over the grounded slab, as detailed in Appendix A. For the design presented in Fig. 2, the values obtained are $L_{\mathrm{s}} = 1.60$ nH, $R_{\mathrm{d}} = 0.17\ \Omega$, $L_{\mathrm{d}} = 1.92$ nH, and $C_{\mathrm{d}} = 0.98$ pF represents the two fringe capacitances at the two sides of each patch toward the ground and toward adjacent patch elements, as shown in Fig. 3 of [22] and Fig.13 of [23].

Once these circuit elements are determined, the varactor is incorporated to complete the RIS unit cell model by adding its RF impedance Z_{v} to the equivalent circuit as shown in Fig. 3. In this configuration, the varactor is physically connected only on one side of the patch toward the ground, and therefore its impedance Z_{v} is in parallel with only one of the two fringe capacitors. Accordingly, the lumped capacitor C_{d} is divided into two series capacitors and, after tuning, fitting the model with full-wave results yields the values $C_{\mathrm{d1}} = 1.25$ pF and $C_{\mathrm{d2}} = 2.72$ pF. We have verified that the model in Fig. 3 with split capacitors C_{d1} and C_{d2} produces more accurate results than considering a single capacitor C_{d} in parallel with the varactor impedance, over the entire range of frequencies and varactor voltages considered. The circuit in Fig. 3 replaces Fig. 4 in [18], where the splitting of the capacitance C_{d} into two separate capacitors, C_{d1} and C_{d2}, was omitted from the figure but accounted for in the numerical results.

The varactor's impedance is modeled by an equivalent series RLC circuit

$$Z_{\mathrm{v}}(V) = R_{\mathrm{v}}(V) + j\omega L_{\mathrm{v}} + \frac{1}{j\omega C_{\mathrm{v}}(V)}, \tag{5}$$

where the variable capacitance $C_{\mathrm{v}}(V)$ and resistance $R_{\mathrm{v}}(V)$ are functions of the reverse-biasing voltage V, and the constant inductance $L_{\mathrm{v}} = 2.39$ nH models both the package inductance and the parasitic inductance introduced when the varactor is soldered across the unit cell gap. The values of $C_{\mathrm{v}}(V)$ and $R_{\mathrm{v}}(V)$ are obtained through a parametric sweep simulation in the commercial Keysight Advanced Design System (ADS) software, based on the SPICE model of the varactor provided by the manufacturer. These values are limited to the reverse voltage bias range of [4 V, 15 V] and are detailed in Table I.

As shown in Fig. 3, the RLC varactor model is connected in parallel to the capacitance C_{d1}, and the total equivalent

TABLE I: Values of C_{v} and R_{v} for the varactor model in Fig. 3 for different values of the varactor biasing voltage.

V (V)	C_{v} (pF)	R_{v} (Ω)
4	0.802	0.509
5	0.697	0.340
6	0.626	0.221
7	0.578	0.142
8	0.544	0.091
9	0.519	0.058
10	0.501	0.037
11	0.488	0.024
12	0.478	0.016
13	0.471	0.011
14	0.465	0.007
15	0.460	0.005

impedance of the RIS is hence given by

$$Z_{\mathrm{RIS}} = \left(R_{\mathrm{d}} + j\omega L_{\mathrm{d}} + \frac{1}{j\omega C_{\mathrm{d2}}} + Z_{\mathrm{v}} \parallel \frac{1}{j\omega C_{\mathrm{d1}}} \right) \parallel j\omega L_{\mathrm{s}}. \tag{6}$$

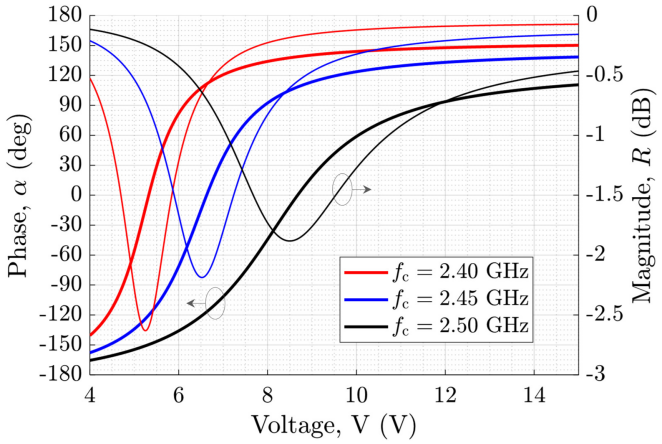
Finally, Z_{RIS} is used to determine the reflection coefficients, Γ, of the RIS elements:

$$\Gamma = \frac{Z_{\mathrm{RIS}} - \eta_0}{Z_{\mathrm{RIS}} + \eta_0}, \tag{7}$$

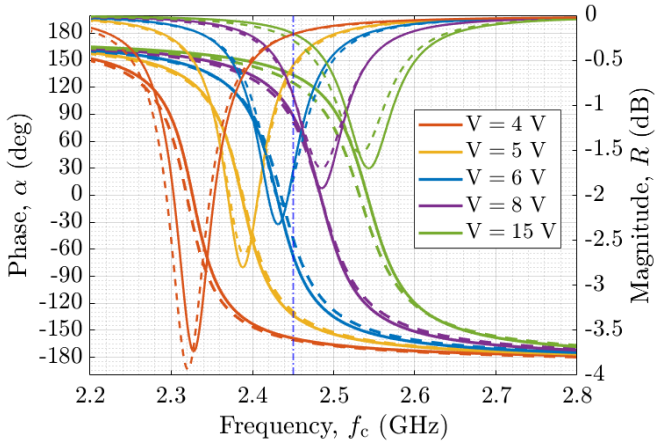
where $\eta_0 = 377\ \Omega$ is the free-space impedance. The magnitude and phase of Γ are denoted by $R(V)$ and $\alpha(V)$, respectively. The values of R and α as functions of the biasing voltage for the unit cell in Fig. 2 are shown in Fig. 4(a) for three different frequencies, including the target RF frequency $f_{\mathrm{c}} = 2.45$ GHz. The voltage V is positive as the varactor is connected in reverse, with its anode grounded and its cathode connected to the positive biasing voltage. At $f_{\mathrm{c}} = 2.45$ GHz, the phase α varies between $-160°$ and $+140°$, with the most significant variations occurring between 4 and 10 V. The lowest reflection magnitude R, approximately -2.4 dB, is observed around 7 V. Fig. 4(b) illustrates the behavior of α and R as functions of the RF frequency and compares the analytical model (solid lines) with full-wave simulations performed using the commercial software CST Studio Suite (dashed lines) for five different biasing voltages. The agreement is generally good across different biasing voltages and frequencies, with particularly strong accuracy at the target frequency $f_{\mathrm{c}} = 2.45$ GHz (dotted line in blue). Although in practical RIS implementations the control is optimized based on channel estimates, having an analytical model is useful for design and research purposes or to assist the optimization algorithms.

In practice, the achievable cell reflection phases are limited by the bias voltage range of the varactor diode. At very low bias voltages, the varactor approaches its forward-conduction region and exhibits increased nonlinearities and losses, while at high reverse-bias voltages the capacitance variation gradually saturates. Consequently, the effective capacitance tuning range is finite, limiting the achievable reflection phases to values smaller than 360°. This limitation can be mitigated by using varactors with larger capacitance tuning ratios, optimizing the unit-cell geometry to increase phase sensitivity, or employing multi-resonant and multi-tunable-element designs [24]–[26].

The model is obtained using periodic boundary conditions for normal incidence. As conventionally done in reflectarrays or RIS metasurfaces, we use the well-accepted "local periodicity" approximation: if the mth varactor has a voltage bias $w(m)$ at $x_m = md_x$ for $m = 0, 1, ..., M-1$, that is slowly varying with m, then the mth reflection coefficient $\Gamma_m = R_m e^{j\alpha_m}$ is well approximated by (7).



(a)



(b)

Fig. 4: Phase and magnitude response of the reflection coefficient for RIS unit cells as a function of (a) the varactor's biasing voltage at three different frequencies, based on the analytical model described by (7), and (b) the frequency at five different biasing voltages. Solid lines represent results from (7) that are in good agreement with full-wave simulations (dashed lines).

B. Biasing Transmission Line Design

The goal is to control the RIS reflection coefficients independently using the BSWs $w_n(x,t)$ in the BTL. After rectification at $x_m = md_x$, control of the dc biasing voltages $w(m)$ leads to control of the reflection magnitudes and phases R_m and α_m on each cell.

The BTL is a printed microstrip meandered line (or serpentine), chosen for its compact size, phase delay control, and ease of fabrication; see Fig. 5. It is made of copper and implemented on a grounded dielectric substrate RO3010 with relative permittivity $\epsilon_r = 11.2$, $\tan\delta = 0.0022$, and thickness $h = 0.64$ mm. The BTL board consists of 27 identical unit cells, where the two cells at the ends have been modified to include SMA connectors that allow connection of the signal generator and integration of possible external loads, if required, to ensure optimal performance within the desired frequency range. The proposed design details and geometry are displayed in Fig. 5. The dimensions of the BTL unit cell are (in mm): $d_x = 20$, $C = 5$, $E = 7.64$, $F = 11$, $G = 1.8$, $H = 50$, $L_\mathrm{p} = 131.42$, $W = 2.6$.

Each unit cell of the BTL has a curvilinear path length L_p and a spatial period d_x along the x direction (the same as for the RIS board), and is connected to a rectifier that extracts the desired dc voltage to bias the varactor located on the RIS board. The BTL signal travels along the microstrip with phase velocity c/n_eff where $n_\mathrm{eff} = \sqrt{\epsilon_\mathrm{eff}} = 2.94$ is the effective refractive index of the microstrip and $\epsilon_\mathrm{eff} = 8.66$ is its effective permittivity, which is approximately calculated as [27]

$$\epsilon_\mathrm{eff} = \frac{\epsilon_r + 1}{2} + \frac{\epsilon_r - 1}{2} \frac{1}{\sqrt{1 + 12h/W}}, \tag{8}$$

and is considered dispersionless in the frequency range of operation. The characteristic impedance of the microstrip is $Z_0 = 19.23\ \Omega$. In this case, the slowness factor, used in (1)-(4), is also determined by the path length L_p and the period d_x, and is given by $n_\mathrm{slow} = n_\mathrm{geom} n_\mathrm{eff}$, where $n_\mathrm{geom} = L_\mathrm{p}/d_x = 6.57$ represents the geometric index that allows for projection of the standing wave pattern from the printed meandered line onto the x direction. Thus, the resulting slowness factor is $n_\mathrm{slow} = 19.34$. Although the segments L_left and L_right of the BTL follow the same meandered line geometry as the main section L, these two additional segments can have a different geometry as they are not connected to any rectifier. However, the values of L_left and L_right must be normalized with respect to the geometric index in order to be used in (1)-(4). Therefore, the total length of the BTL along the x direction is $L_\mathrm{tot} = 540$ mm, with $L = 520$ mm, and $L_\mathrm{left} = L_\mathrm{right} = 0.5d_x = 10$ mm, while the total path length of the meandered microstrip is 3548.3 mm.

Using a printed meandered microstrip topology for the BTL design offers the significant advantage of increasing the slowness of the waves in the x direction, allowing the use of low frequencies for the BSWs. This advantageous feature helps mitigate unwanted interference from the BTL harmonics on the RF system. The scattering parameters have been analyzed to assess the losses and reflection performance of the BTL design. The selected frequency range spans from 0 to 300 MHz, which is much lower than the RF band (here, around 2.45 GHz). When the RIS is used with several standing waves, as in [13], [16], this design allows for a fundamental frequency of approximately 7.18 MHz. This ensures that at least 21 modes are available below 300 MHz, which is a sufficient number of degrees of freedom for RIS control. The frequency f_b of the fundamental BSW decreases when the number M of RIS elements increases. Fig. 6 presents the transmission coefficient of the BTL design (without considering the losses of the 27 rectifiers), obtained from a full-wave simulation in CST Studio Suite. The results show a gradual decrease with frequency due to ohmic and dielectric losses, reaching a minimum value of -2.44 dB at 300 MHz. Although not depicted in the figure, the reflection coefficient with Port 2 matched to its characteristic impedance remains consistently

below -34 dB across the entire frequency range, indicating minimal mismatch. The BSWs are formed along the BTL due to an open or short termination at $x = -L_{\text{left}}$.

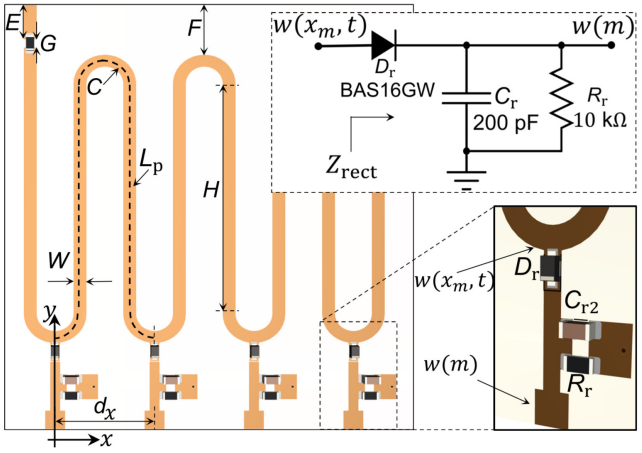


Fig. 5: Geometry of the BTL formed by a meandered microstrip line over a grounded dielectric layer (not shown). The rectifiers of the ac BSW are at the bottom of the figure, one per RIS element. The voltages $w(x_m, t)$, $m = 0, 1, ..., M-1$ are obtained from the lower portion of the BTL. The node of the rectified voltage $w(m)$ is subsequently connected to the coplanar waveguide on the RIS board (connection not shown here).

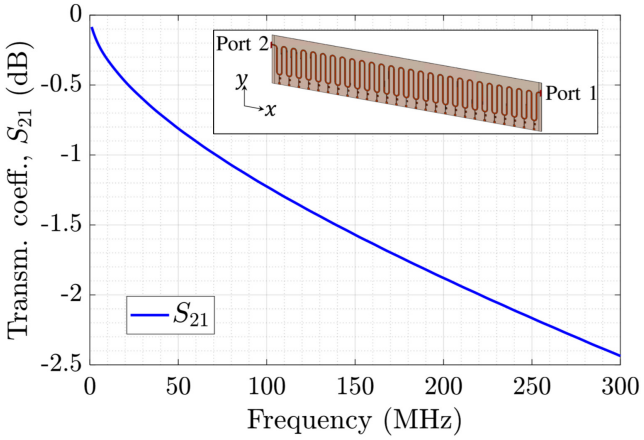


Fig. 6: Transmission coefficient S_{21} of the BTL with $M = 27$ elements for a frequency range of 0 to 300 MHz. The value of S_{21} decreases with frequency, reaching -2.44 dB at 300 MHz. The lowest frequency of the BSW in this paper is $f_b = 7.18$ MHz.

To extract the dc voltages $w(m)$ from the BTL standing wave $w(x_m, t)$ at each $x_m = md_x$ location, a rectifier circuit composed of a resistor R_r, a capacitor C_r, and a diode D_r was designed. The capacitor and the resistor are grounded via a through-hole as shown in Fig. 5 (only the microstrip layer is shown, the ground plane underneath is not shown), while the diode is connected between these components and the BTL at position x_m. The ADS time-domain circuit simulator was employed to optimize the design of the circuit, resulting in $R_r = 10$ kΩ and $C_r = 200$ pF. To mitigate RF current effects on both boards, the capacitor C_r is implemented as two 100-pF capacitors in parallel: C_{r1} on the RIS board (see Fig. 2) and C_{r2} on the BTL board. The BAS16GW diode provided by Nexperia was selected for its fast recovery time of 4 ns and low capacitance of 1.5 pF. By choosing a time constant of $\tau = 2$ μs, the rectifier effectively tracks signal peaks, as shown in Appendix B, while maintaining the impedance Z_{rect} seen by the BTL between a few hundred and 1000 Ω for frequencies up to 300 MHz. However, this is not a constant linear impedance as the diode admittance depends on its instantaneous voltage and conduction state. Although these values exceed Z_0, the loading of 27 nonlinear branches reduces the standing-wave envelope, as quantified in Sec. IV-C. The selected rectifier and diode are proof-of-concept choices rather than globally optimized components. Fig. 5 illustrates the rectifier circuit (inset) and its connection to the BTL and the RIS board. Further analysis of the rectifier temporal response is discussed in Appendix B.

Fig. 7 shows the BTL and its connection to an arbitrary waveform generator (AWG), modeled with an ideal ac power supply V_g in series with an impedance Z_g, a dc power supply $V_{dc} = W_0$, rectifiers, and some decoupling elements, detailing the current flow of the ac and dc signals. Due to the need for the offset voltage W_0, decoupling the ac and dc signals is necessary to prevent short-circuiting and ensure proper current flow along the BTL. To achieve this, a capacitor $C_f = 1$ μF is connected after the AWG to act as a high-pass filter, while an inductor $L_f = 680$ μH is inserted after the dc power supply to serve as a low-pass filter. An additional capacitor C_f is connected between the end of the BTL and either a short or open-circuit termination. The chosen capacitors provide a capacitive reactance $X_{Cf} \approx 0.3$ Ω at 500 kHz, while the chosen inductor offers an inductive reactance $X_{Lf} \approx 2.1$ kΩ at the same frequency. This setup ensures that ac signals above 500 kHz (i.e., including all biasing modes) flow through the capacitors but not through the inductor, while signals below 500 kHz (i.e., the dc biasing voltage W_0) flow through the inductor but not the capacitors, avoiding short circuits at the opposite end of the BTL.

Since the varactors are connected in reverse bias, the current through them is negligible. Unlike the dc current, the ac current also reaches the BTL termination through the coupling capacitor C_f. Therefore, the maximum expected dc current flowing from the dc power supply depends on the number of elements M, the constant voltage W_0, and the resistance R_r. In this case, assuming that the diode D_r is lossless, the expected dc current is $I_{dc} = 27(4/10000) = 10.8$ mA.

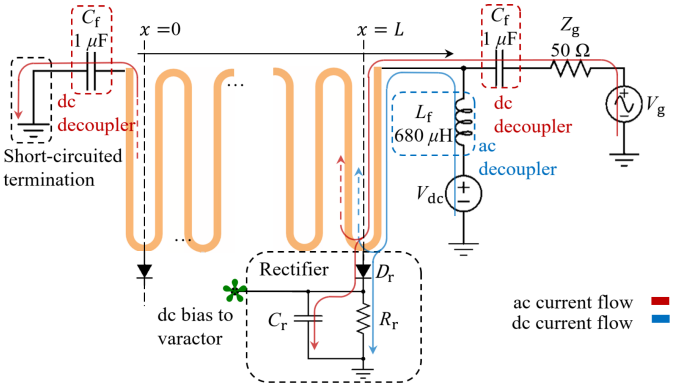


Fig. 7: BTL circuit including connections to the rectifiers, AWG, and dc power supply, as well as the circuit elements required for ac and dc signal decoupling. The flow of the ac (red) and dc (blue) currents along the BTL and through each rectifier is also shown.

IV. Analysis and Experimental Validation of the DC Bias Distribution

A. Effects of BTL Termination and Impedance Matching

To attain the full capabilities of the wave-controlled RIS, the maximum value of the voltage $w(m)$ measured after the rectifiers must be high enough to enable the widest possible reflection phase range. This voltage amplitude is influenced by proper selection of the frequency f_b and the BTL termination, either short- or open-circuited. For a short-circuited termination at $x = -L_\mathrm{left}$, the input impedance at $x = L + L_\mathrm{right}$ is given by $Z_\mathrm{in} = jZ_0\tan(\kappa)$, where Z_0 is the characteristic impedance of the microstrip and $\kappa = (\omega_\mathrm{b} n_\mathrm{slow}/c)L_\mathrm{tot}$. In the particular case where $f_\mathrm{b} = nf_{\mathrm{b},0}$, with $n = 1, 2, 3, ...$, and $f_{\mathrm{b},0}$ is chosen such that the wavelength $\lambda_{\mathrm{b},0} = c/(n_\mathrm{slow} f_{\mathrm{b},0}) = 4L_\mathrm{tot}$, the input impedance is $Z_{\mathrm{in},n} = jZ_0\tan(n\pi/2)$. Under this condition, $Z_{\mathrm{in},n}$ becomes infinite for odd multiples of $f_{\mathrm{b},0}$ (i.e., $n = 1, 3, 5, ...$), and zero for even multiples (i.e., $n = 2, 4, 6, ...$). As a result, the voltage at $x = L + L_\mathrm{right}$ reaches a maximum for odd multiples and a minimum for even multiples of $f_{\mathrm{b},0}$.

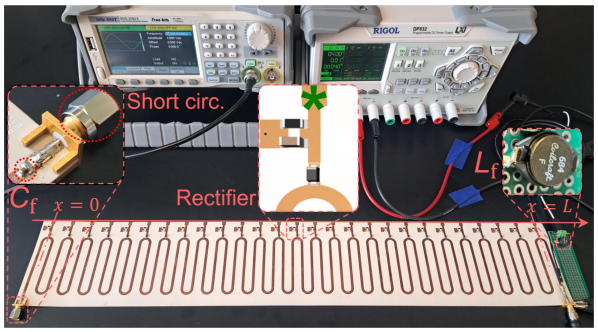


Fig. 8: Printed meandered BTL backed by the grounded dielectric substrate RO3010 connected to the Siglent SDG6052X AWG and the RIGOL DP832 dc power supply.

In order to experimentally compare the voltage distribution along the BTL for even and odd multiples of $f_{\mathrm{b},0}$, we use the experimental setup shown in Fig. 8, which includes an AWG, power supply, decoupling elements, and BTL. For the BTL design presented here, $f_{\mathrm{b},0} = 7.18$ MHz. With an AWG modeled as an ideal ac source with $V_\mathrm{g} = 10$, Fig. 9 shows the voltages $w(m)$ for six BSWs with frequencies that are multiples of $f_{\mathrm{b},0}$. These voltages are measured using a dc-coupled SIGLENT SDS2104X Plus digital oscilloscope and an Agilent N2863B 10:1 passive probe (dc-300 MHz, 10 MΩ, and 15 pF) at positions $x_m = md_x$, $m = 0, 1, ..., M-1$, after each rectifier, with the BTL terminated in a short circuit. The results reveal a maximum amplitude difference exceeding 3 V between odd and even multiples of $f_{\mathrm{b},0}$. However, the minimum values remain close to W_0 in all cases, slightly falling below W_0 due to losses associated with the rectifiers. The voltages at the first and last elements show slight deviations from the expected values, with these deviations increasing at higher frequencies since the measurements were taken half a period $(d_x/2)$ before the ends of the BTL, corresponding to the lengths of L_left and L_right.

Similarly, for the case where the BTL is terminated in an open circuit at $x = -L_\mathrm{left}$, the input impedance at

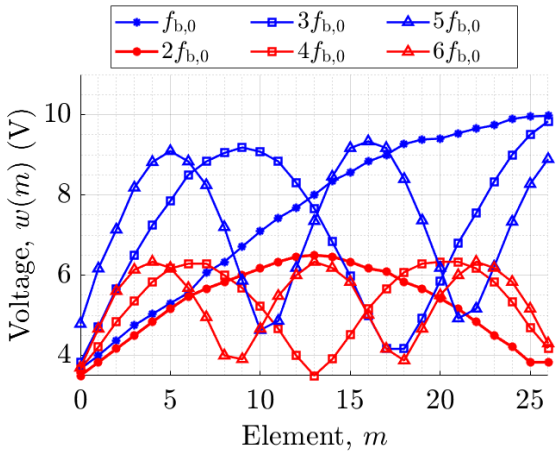


Fig. 9: Measured dc bias voltage $w(m)$ along the BTL at positions $x_m = md_x$ for six individual BSWs, with the BTL terminated by a short circuit at $x = -L_\mathrm{left}$. The red and blue curves represent cases where f_b is an even or odd multiple of $f_{\mathrm{b},0}$, respectively.

$x = L + L_\mathrm{right}$ is $Z_\mathrm{in} = jZ_0\cot(\kappa)$. By choosing $f_\mathrm{b} = nf_{\mathrm{b},0}$ as before, the input impedance for the n-multiples of $f_{\mathrm{b},0}$ becomes $Z_{\mathrm{in},n} = jZ_0\cot(n\pi/2)$. This causes $Z_{\mathrm{in},n}$ to become infinite for even multiples of $f_{\mathrm{b},0}$ and zero for odd multiples, resulting in a maximum voltage at $x = L + L_\mathrm{right}$ for even multiples of $f_{\mathrm{b},0}$ and a minimum for odd multiples. Fig. 10 presents a comparison of the voltages $w(m)$ measured along the BTL with an open-circuit termination. Similar to previous cases, the results reveal a maximum amplitude difference of over 3 V between odd and even multiples of $f_{\mathrm{b},0}$, with higher amplitudes for even multiples in this case. As before, the minimum values remain close to W_0 for all cases, while slight deviations are observed in the first and last elements due to the $d_x/2$ shift before the BTL endpoints.

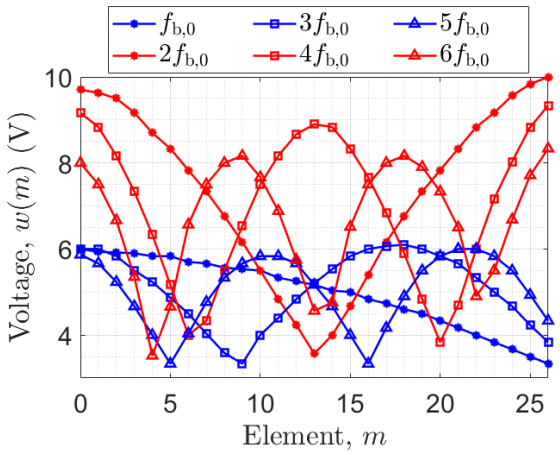


Fig. 10: Similar to Fig. 9, but with the BTL terminated by an open circuit at $x = -L_\mathrm{left}$.

The difference observed in the amplitude for open- and short-circuited terminations is attributed to the effect of the output impedance Z_g of the AWG that injects the periodic time-domain signal at $nf_{\mathrm{b},0}$. As an example, Fig. 11 shows the maximum dc biasing voltage $w_\mathrm{max} = \max_m w(m) = W_\mathrm{b} + W_0$ versus the frequency f_b for a few values of the AWG impedance Z_g from Z_0 (19.23 Ω, red curve) to 100 Ω (green curve), assuming a short-circuit termination. These

results are obtained using an analytical model of the BTL.

We observe that for frequencies that are odd multiples of $f_{\mathrm{b},0}$, $w_{\max}$ remains constant and reaches its largest possible value. On the contrary, for frequencies that are even multiples of $f_{\mathrm{b},0}$, $w_{\max}$ varies depending on the impedance of the AWG. This behavior arises because the relationship $W_{\mathrm{b}} = (Z_0/Z_{\mathrm{g}})V_{\mathrm{g}}$ applies for even multiples of $f_{\mathrm{b},0}$, while for odd multiples we have $W_{\mathrm{b}} = V_{\mathrm{g}}$. Consequently, to maximize $w_{\max}$ for *both* even and odd multiples of $f_{\mathrm{b},0}$, the BTL should be designed with a characteristic impedance Z_0 that matches the AWG impedance Z_{g}. The mathematical derivations supporting this analysis are provided in Appendix C.

In summary, from a practical perspective, two different design criteria can be employed to maximize $w_{\max}$ and ensure that it remains constant for all frequencies. The first approach involves selecting $f_{\mathrm{b}} = nf_{\mathrm{b},0}$ with n odd, which guarantees maximization regardless of the relationship between Z_{g} and Z_0. For the second approach, the BTL is designed with $Z_0 = Z_{\mathrm{g}}$, which ensures maximization of $w(m)$ for every value of f_{b}. The second approach offers an additional advantage when multiple BSWs are used [16], as it effectively doubles the number of biasing modes within the same frequency range while also making f_{b} independent of the total length L_{tot}. This impedance relationship therefore impacts the selection of n_{slow}, which must balance propagation losses, impedance matching, and enough spectral separation between the BSW frequencies and the RIS operating band.

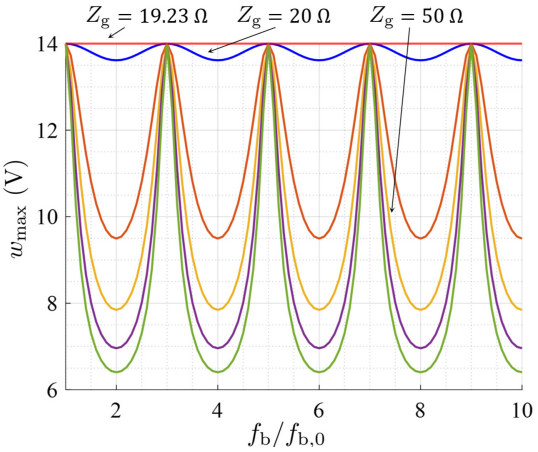


Fig. 11: Maximum dc biasing voltage along the BTL for different frequencies for a short-circuit BTL termination, assuming $V_{\mathrm{g}} = 10$ V and Z_{g} between Z_0 (red curve) and 100 Ω (green curve). When $Z_{\mathrm{g}} = Z_0$, the maximum voltage is the same for even and odd multiples of $f_{\mathrm{b},0}$.

B. Comparison with Circuit–Electromagnetic Co-Simulation

In addition to the analytical model, a circuit-electromagnetic co-simulation of the BTL was developed in ADS. As shown in Fig. 12, the AWG was modeled as an ideal ac source with $V_{\mathrm{g}} = 10$ V followed by an explicit series output resistance $Z_{\mathrm{g}} = 50$ Ω. The ideal dc power source provides $V_{\mathrm{dc}} = W_0 = 4$ V, and the ac and dc excitations are combined through the decoupling capacitor $C_{\mathrm{f,right}}$ and RF choke $L_{\mathrm{f,right}}$, respectively. Adjacent rectifier connection points are connected by identical two-port Touchstone models of one BTL unit cell, extracted from a full-wave CST simulation that includes the actual conductor geometry, substrate properties, conductor and dielectric losses, and electromagnetic coupling. The two ends of the cascade are completed by half-unit-cell two-port Touchstone models of lengths $L_{\mathrm{left}} = L_{\mathrm{right}}$. Each of the M BTL segments is loaded by an identical rectifier comprising a BAS16GW diode, R_{r}, and C_{r}. The diode is represented by the vendor-provided Nexperia SPICE3 subcircuit, a compact nonlinear diode model. The remaining lumped components C_{f}, L_{f}, R_{r}, and C_{r} are modeled by their ideal nominal values. At the left boundary, $C_{\mathrm{f,left}}$ is either grounded, yielding $Z_{\mathrm{L}} = 1/(j\omega C_{\mathrm{f,left}}) \approx 0$ at the BSW frequencies, or left floating to approximate an open circuit. Both decoupling capacitors have the same nominal value, $C_{\mathrm{f,left}} = C_{\mathrm{f,right}} = C_{\mathrm{f}}$.

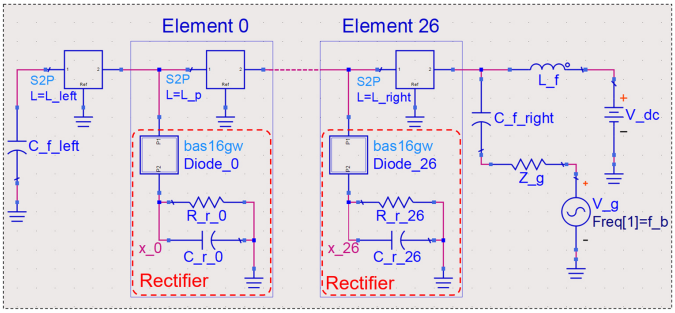


Fig. 12: ADS circuit-electromagnetic co-simulation of the $M = 27$-element BTL. Full-UC and half-UC Touchstone blocks model the distributed line, while each element includes its nonlinear rectifier. The right-hand bias tee combines the ac and dc sources, and the left-hand capacitor provides an approximate RF short when grounded.

In the two CST models used to extract the Touchstone blocks for the full and half BTL unit cells, a 5 mm uniform microstrip extension was placed between each wave port and the nearest curved section. These extensions allow the port mode to settle before reaching the bend and reduce direct interaction between the port boundary and the discontinuity. The port reference planes were shifted to the extensions, thereby de-embedding propagation through the 5 mm access lines. Consequently, the exported scattering parameters represent only the intended full or half unit cells between the indicated reference planes. Over the plotted $0 - 300$ MHz band, the transmission coefficient remains above approximately -0.10 dB for the full unit cell and -0.05 dB for the half unit cell, consistent with the low-loss BTL response reported in Fig. 6.

Fig. 13 compares the voltage $w(m)$ evaluated using the ADS model with experimental results for two different BSW frequencies: one using an even multiple of $f_{\mathrm{b},0}$ and the other using an odd multiple, both with a short-circuit termination. The co-simulation reproduces the measured spatial periodicity and locations of the voltage extrema for both cases. This agreement is enabled by the full-wave unit cell models, which include the meander curvature, distributed loss, and intra-unit-cell coupling absent from the ideal formulation. The remaining amplitude differences are addressed in the next subsection by separating the effects of the BTL and fixtures from those of the distributed rectifier loading.

Fig. 14 compares the reflection phase α_m obtained by mapping the ADS and the measured voltages through the voltage-dependent unit-cell response in Fig. 4(a). For $2f_{\mathrm{b},0}$,

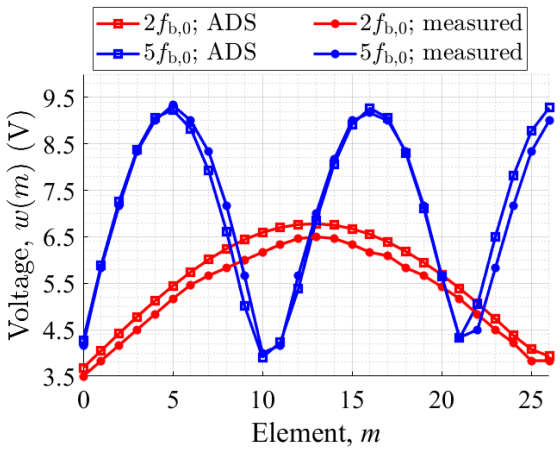


Fig. 13: Rectified voltage distribution along the BTL for single-tone excitation at $2f_{\mathrm{b},0}$ and $5f_{\mathrm{b},0}$ where $W_{\mathrm{b}} = V_{\mathrm{g}} = 10$ V and $W_0 = V_{\mathrm{dc}} = 4$ V.

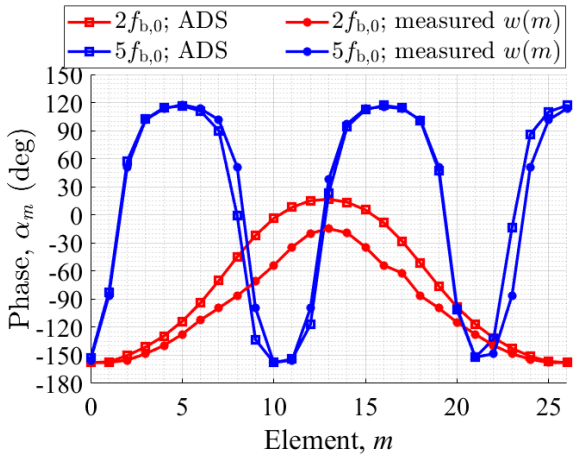


Fig. 14: Reflection-phase distribution along the linear RIS array obtained from the ADS and measured rectified voltages for single-tone excitation at $2f_{\mathrm{b},0}$ and $5f_{\mathrm{b},0}$.

the measured phase varies from around $-150°$ to $-15°$, while the ADS result reaches about $25°$ near the center of the array, resulting in only moderate agreement. For $5f_{\mathrm{b},0}$, both results reproduce the two complete spatial periods of the phase distribution, spanning approximately $-150°$ to $120°$, with localized voltage-related discrepancies that become more pronounced in the remaining half-period. These discrepancies can be appreciably larger than the corresponding voltage differences because the nonlinear mapping $\alpha(w)$ amplifies a voltage error Δw_m by approximately $\Delta\alpha_m \simeq (\mathrm{d}\alpha/\mathrm{d}w)_{w(m)}\Delta w_m$, particularly where $|\mathrm{d}\alpha/\mathrm{d}w|$ is large, which in this case occurs near 6.5 V (where $\alpha = 0°$), as shown in Fig. 4(a). Nevertheless, despite its larger phase excursion, the ADS and measured patterns agree better for $5f_{\mathrm{b},0}$, indicating that phase errors perturb the effective gradient and coherence less severely than for $2f_{\mathrm{b},0}$.

The corresponding reflected-field factor for normal plane-wave incidence is

$$F(\theta) = \frac{1}{M}\sum_{m=0}^{M-1} R_m e^{jmkd_x \sin(\theta)+j\alpha_m}, \tag{9}$$

where α_m and R_m, previously shown in Fig. 4(a), represent the phase and magnitude of the reflection coefficient for the m-th unit cell given the applied voltage $w(m)$, as determined by (4). As shown in Fig. 15, the principal reflected fields occur near broadside for $2f_{\mathrm{b},0}$ and near $\theta = \pm 32°$ for $5f_{\mathrm{b},0}$. The ADS- and measurement-based calculations preserve these principal directions, while differing more noticeably in null depth and sidelobe level for $2f_{\mathrm{b},0}$.

The effect of a phase discrepancy depends on its spatial distribution across the array. A common phase offset does not change the pattern magnitude, whereas a linearly varying error modifies the phase gradient and shifts the beam. Nonuniform errors reduce coherent addition, potentially lowering the main-beam gain and modifying its width, sidelobes, and nulls; errors approaching $180°$ can produce locally destructive contributions. Equation (9) captures these spatially dependent effects directly from the simulated or measured element voltages.

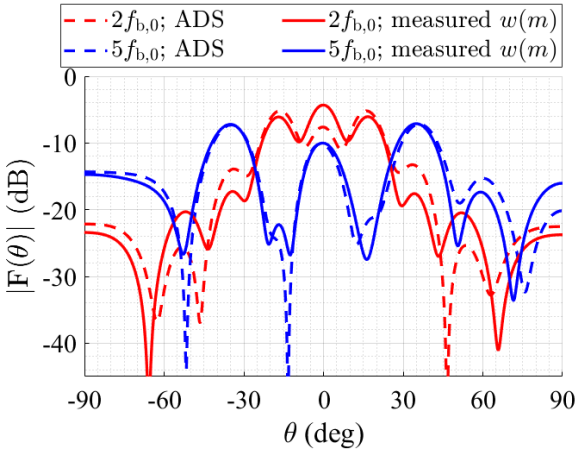


Fig. 15: Reflected radiation pattern calculated from the ADS and measured voltage distributions for normal plane-wave incidence and single-tone BTL excitation at $2f_{\mathrm{b},0}$ and $5f_{\mathrm{b},0}$.

C. Origin of the Differences Among the Analytical, Circuit-Level, and Experimental Results

The analytical model assumes an ideal, nonloading peak detector, whereas the ADS co-simulation includes the full-wave unit cell model, bias network, and nonlinear rectifiers, and the measurements additionally include hardware and instrumentation nonidealities. To separate these contributions, additional ADS simulations and measurements were performed with all diodes connected to the BTL (loaded case) and with the diode-BTL connections open (diode-disconnected case). The probe 10:1 (10 MΩ ‖15 pF) may also perturb the BSW, particularly at $5f_{\mathrm{b},0}$, where its capacitive reactance decreases from approximately 740 Ω to 296 Ω.

To distinguish the practical voltages from $w(m)$ in (2), let $w_{\mathrm{pk,nr}}(m)$ and $w_{\mathrm{pk,r}}(m)$ denote the steady-state ac peak input voltages at the position of the m-th rectifier without and with the rectifier connected, respectively. In contrast, $w(m)$ denotes the dc output across C_{r}; ideally, it equals the peak predicted by (2). The loading and rectification differences are therefore

$$\begin{aligned} \Delta w_{\mathrm{load}}(m) &= w_{\mathrm{pk,r}}(m) - w_{\mathrm{pk,nr}}(m), \\ \Delta w_{\mathrm{rect}}(m) &= w_{\mathrm{pk,r}}(m) - w(m). \end{aligned} \tag{10}$$

Here, Δw_{load} quantifies the change in the local BTL ac peak caused by rectifier loading, whereas Δw_{rect} accounts for the total nonideal rectification, from ac to dc, including the diode drop, series resistance, capacitor discharge, ripple, leakage, and parasitic effects. For an ideal, nonloading rectifier, $\Delta w_{\mathrm{load}}(m) = \Delta w_{\mathrm{rect}}(m) = 0$, recovering (2).

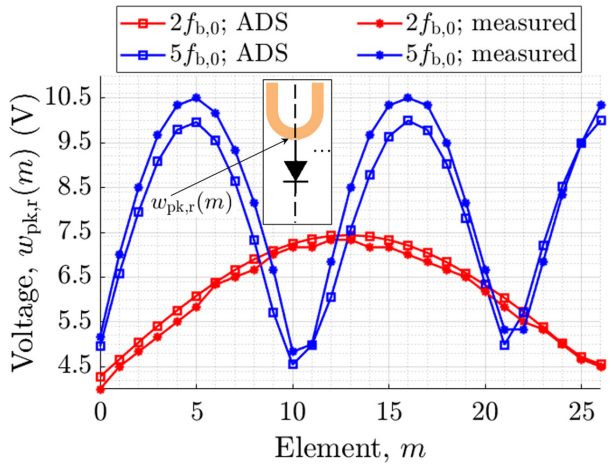


Fig. 16: Peak voltage $w_{\mathrm{pk,r}}(m)$ immediately upstream of each rectifier for the loaded BTL at $2f_{\mathrm{b},0}$ and $5f_{\mathrm{b},0}$: ADS co-simulation and measurement.

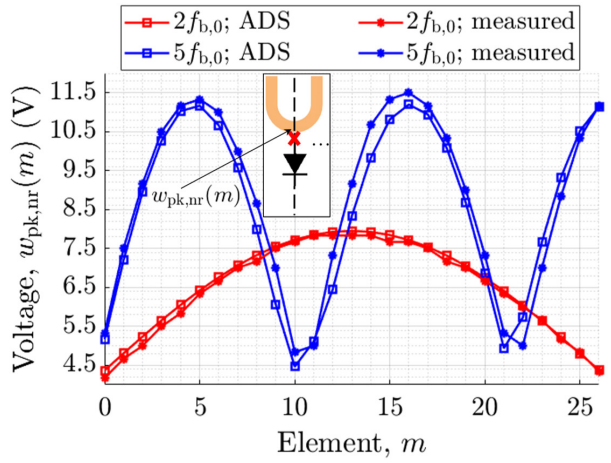


Fig. 17: Peak voltage $w_{\mathrm{pk,nr}}(m)$ at the corresponding BTL nodes after opening the rectifier diode-BTL connections, for $2f_{\mathrm{b},0}$ and $5f_{\mathrm{b},0}$: ADS co-simulation and measurement. In the measured configuration, the rectifier pads and interconnect traces remain on the board.

Figures 16 and 17 compare the peak voltages for the rectifier diode-connected and rectifier diode-disconnected cases, respectively. In the diode-disconnected case, ADS closely reproduces both the measured extrema positions and their amplitudes at the two BSW frequencies. This result indicates that the cascaded full-wave unit cell models describe the dominant propagation, dispersion, and loss mechanisms of the BTL. The larger residual difference in the diode-connected case, particularly around the maxima at $5f_{\mathrm{b},0}$, points to the rectifier branches and their interconnects as the dominant additional source of model uncertainty. Residual differences can arise from the ideal models used for C_{f} and L_{f}, structures outside the CST reference planes, probe capacitance, the residual pads and traces in the diode-disconnected hardware, and coupling across cascaded two-port boundaries. The full-wave UC blocks capture local coupling, but the cascaded model does not isolate shared-ground and dc-return coupling.

Figure 18 compares the three measured quantities at $5f_{\mathrm{b},0}$. The difference between $w_{\mathrm{pk,nr}}(m)$ and $w_{\mathrm{pk,r}}(m)$ directly reveals the rectifier-induced loading on the ac signal, whereas the separation between $w_{\mathrm{pk,r}}(m)$ and $w(m)$ represents the total rectification loss $\Delta w_{\mathrm{rect}}(m)$, from ac to dc. Near the voltage minima, $w_{\mathrm{pk,r}}(m)$ and $w_{\mathrm{pk,nr}}(m)$ nearly coincide, indicating weak local loading, while their separation from $w(m)$ shows that nonideal rectification remains significant. The extrema occur at nearly the same element indices in all three curves, indicating that the rectifiers primarily modify the voltage envelope and only weakly perturb the BSW electrical length.

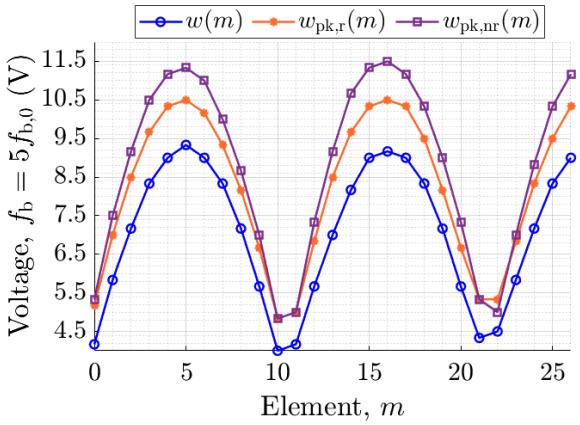


Fig. 18: Measured voltage distributions at $5f_{\mathrm{b},0}$: rectified dc output $w(m)$, peak voltage with the diodes connected $w_{\mathrm{pk,r}}(m)$, and peak voltage with the diode-BTL connections opened $w_{\mathrm{pk,nr}}(m)$.

The absolute separations in Fig. 18 are larger near the BSW maxima than near its minima. This behavior is consistent with peak-detector operation: near a positive voltage crest, the diode conducts in a short current pulse that replenishes C_{r}, and the associated nonlinear conductance, junction capacitance, and series resistance load the BTL. Near a BSW minimum, the ac excursion is smaller and the diode remains below forward conduction for a larger fraction of the period, reducing the absolute conduction-induced loading. Thus, the rectifiers cannot be treated as passive voltage observers; their distributed, time-varying admittances modify the waveform from which the dc control voltage is generated.

Despite these nonidealities, the measurements and co-simulations preserve the principal spatial periodicity and the locations of the BSW extrema predicted by the analytical model. The results therefore validate the proposed wave-controlled biasing proof-of-concept mechanism while demonstrating that accurate prediction of the available control-voltage range requires both the full-wave BTL response and the nonlinear distributed loading of the rectifier network.

V. Reflective Control Using a Single Biasing Frequency

We study the beam- and null-steering capabilities of the wave-controlled RIS with a *single biasing frequency*, as visualized in Fig. 19. Although using a single biasing frequency

does not allow for the more flexible reflective control permitted by multiple BSWs along the transmission line [16], it will be shown that this strategy can be used for reflective control in the following ways: first, for creating nulls at broadside, e.g., to minimize interference reflections, and second, for single beam steering, with limitations at large angles. Further possibilities for extending this control will also be discussed.

The radiation pattern plots in the analysis below result from the proposed design assuming the BTL is lossless and impedance-matched to the AWG, but the analysis applies in more general settings as well. These assumptions allow (4) to be used to determine the exact voltage seen at different points along the BTL. It is important to note that when the BTL is impedance-matched to the AWG, the length of the BTL to the right of the last unit cell, L_{right}, has no impact on the voltage pattern seen by the element rectifiers.

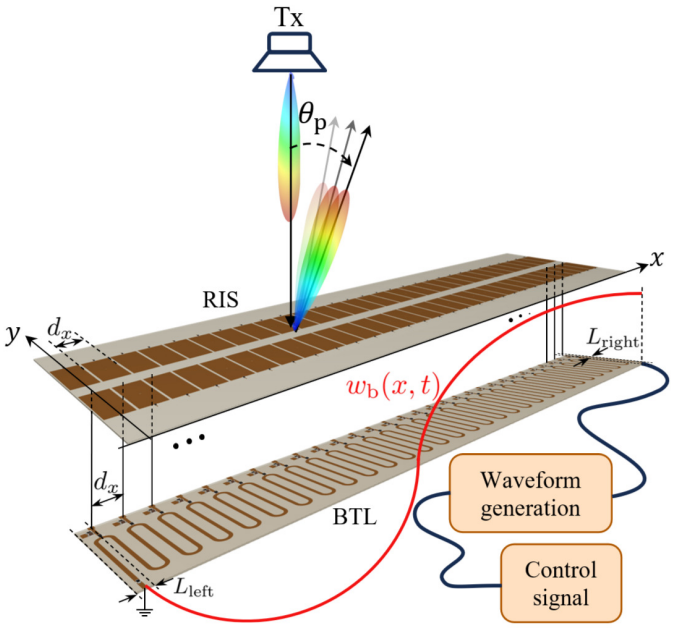


Fig. 19: Wave-controlled RIS consisting of two boards, as described in [13]. The top layer contains M pairs of RIS elements arranged in a row along the x direction, each connected to a varactor diode. In the bottom layer, a single BSW propagates along the BTL, generating the biasing voltages $w(m)$, which are sampled at positions spaced by d_x in the x direction.

A. Nulling the Specular Reflection

For many applications, including those described in [28] and [29], it is necessary to reduce the specular reflection of the incident radiation. Maximizing the reflection towards a different direction does not necessarily fully diminish the specular reflection, due to the non-perfect phase gradient along the RIS. The wave-controlled RIS with multiple BSWs described in [16] was able to suppress the specular component by explicitly including it as a constraint in its optimization criteria. The wave-controlled RIS with a single biasing frequency can also reduce the specular reflection, but with more limited degrees of freedom.

Fig. 20(a) shows the RIS reflection at $\theta = 0°$ for the above design due to normal incident illumination against the biasing frequency f_{b} and the wave amplitude W_{b} in (4). The dc bias, W_0, is not considered to be a tunable parameter here and is set

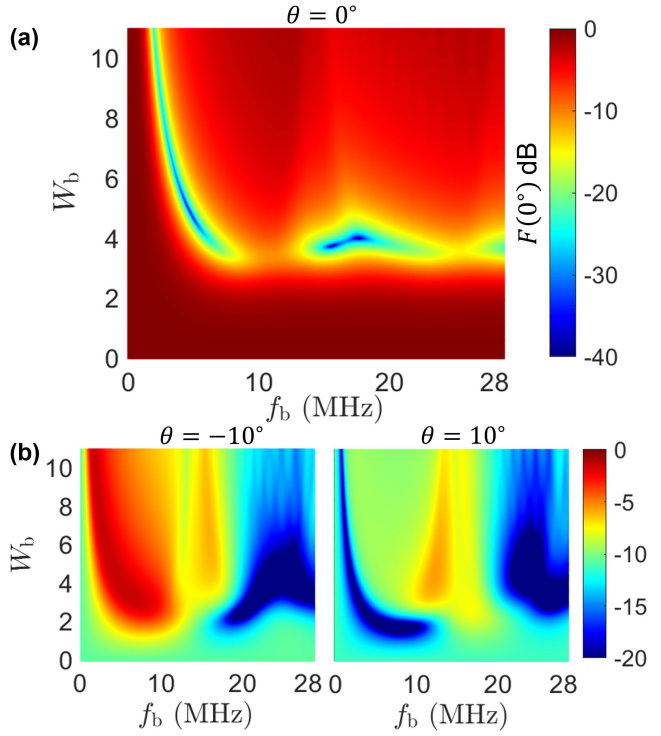


Fig. 20: Colormap of normalized RIS array factor plotted against BSW frequency f_{b} and amplitude W_{b}, with the BTL terminated in a short circuit. We assume normal incidence. (a) Radiation at $\theta = 0°$: minimal specular reflections occur for frequencies f_{b} greater than 7 MHz around $W_{\text{b}} = 4$ V. (b) Radiation at $-10°$ is maximized for frequencies below 10 MHz. The colormap for $10°$ shows no symmetrical "ghost" beam when the beam is directed towards $-10°$.

to 4 V, as this is the minimum biasing voltage required for the varactor specified in this design (see Table I), and increasing the dc bias will reduce the range of controllable phases. From this colormap, it can be seen that for most combinations of frequency and wave amplitude, the specular reflection at $\theta = 0°$ is non-negligible. However, there are combinations of these parameters that result in significantly reduced specular reflection. The region of reduced reflection begins at 2 MHz with $W_{\text{b}} = 12$ V, and is approximately constant at $W_{\text{b}} = 4$ V for frequencies larger than 7 MHz, although the magnitude fluctuates with frequency. The minimal reflections occurring for $W_{\text{b}} = 4$ V coincide with the approximately linear region of the voltage-to-phase relationship shown in Fig. 4(a).

The region of minimal specular reflection results in the radiation being directed elsewhere, as seen by comparing Figs. 20(a) and 20(b), where we observe radiation at $\theta = \pm 10°$. Fig. 20(b) shows that the redirected radiation at $\theta = -10°$ is maximized for frequencies lower than 10 MHz without a symmetric peak at $\theta = 10°$; the symmetric peak often arises with beams steered to larger angles [30].

B. Single Beam Control Near Broadside

For single beam control, the ideal phase difference between adjacent RIS elements is

$$\alpha_{m+1} - \alpha_m = -2\pi d_x \sin(\theta_{\text{p}})/\lambda_{\text{c}}, \tag{11}$$

TABLE II: Values of f_b and W_b for the curves in Fig. 21.

	Short-circuit termination				Open-circuit termination		
	θ_p	f_b (MHz)	W_b (V)		θ_p	f_b (MHz)	W_b (V)
(a)	-4°	1.2	7.3	(b)	4°	8.1	1.8
	-8°	6.0	2.9		8°	7.5	2.7
	-12°	2.0	10.8		12°	7.5	3.7
(c)	-2°	0.7	6.2	(d)	2°	3.6	1.9
	-4°	2.5	3.23		4°	3.4	2.9
	-6°	0.5	10.4		6°	3.5	4.0

where θ_p is the desired beam angle (peak radiation direction) and λ_c is the free-space wavelength of the carrier [31]. Hence, the phase for the element at $x_m = md_x$ on the BTL is

$$\alpha_m = \alpha_0 - 2\pi x_m \sin(\theta_\mathrm{p})/\lambda_\mathrm{c}. \tag{12}$$

For large angles, achieving this phase gradient across the RIS leads to phase wrapping. However, for small angles where $|\alpha_{M-1} - \alpha_0| < 360°$, which do not lead to phase wrapping, this linear phase response along the RIS can be created by a single BSW. This method works best when L_left is small, as it allows for maximum phase variation across the elements. This also follows from the discussion in Sec. IV, as the length L_right does not impact the voltage pattern seen by element $M-1$ when the BTL is impedance matched to the AWG.

There are two aspects of this design that limit the linear phase gradient from being exactly reproduced across the board. The first is the nonlinearity of the voltage-to-phase relationship as seen in Fig. 4(a). This problem can be addressed by using a wideband unit cell design that has a more linear voltage-to-phase relationship, such as the dual resonant element presented in [25]. The second factor is the sinusoidal nature of the voltage gradient across L. For the short-circuit termination, the voltage gradient is approximately linear when $(2\pi f_\mathrm{b} n_\mathrm{slow}(x_{M-1} + L_\mathrm{left}))/c \ll 1$, allowing the small-angle approximation to be applied to (4). Beyond this limit and for either termination, linearity diminishes, but the phase gradient is still monotonically increasing or decreasing along the BTL while $\lambda_\mathrm{b} > 4(L+L_\mathrm{left})$. This condition still allows for a highly directive beam with relatively low sidelobes and a minor loss of power at progressively larger angles, as seen in Fig. 21. The wavelength $\lambda_\mathrm{b} > 4(L+L_\mathrm{left})$ will limit the maximum allowed θ_p as it corresponds to the case where $|\alpha_{M-1} - \alpha_0| < 360°$. Beyond this limit, when $\lambda_\mathrm{b} < 4(L+L_\mathrm{left})$, the phase gradient is no longer monotonic, leading to the generation of other radiation peaks, specifically in the $-\theta_\mathrm{p}$ direction.

Due to these limitations, a trade-off exists between the length of the array, L, and the maximum usable angle for beam steering, θ_p. Larger arrays will have smaller beamwidths but will be more limited in beam steering angles. This is shown in Fig. 21, which illustrates two beam steering examples for both the open- and short-circuit terminations for a wave-controlled RIS with either 27 or 60 elements. At the specified angles, optimal f_b and W_b are obtained through a search of the parameter space (see Table II), while $\theta_\mathrm{p} = 0°$ is maximized when $W_\mathrm{b} = 0$ for any frequency. All of the patterns shown in the figure maintain the $|\alpha_{M-1} - \alpha_0| < 360°$ requirement since the radiation patterns for larger θ_p would have rapidly decreasing directivity in the desired direction.

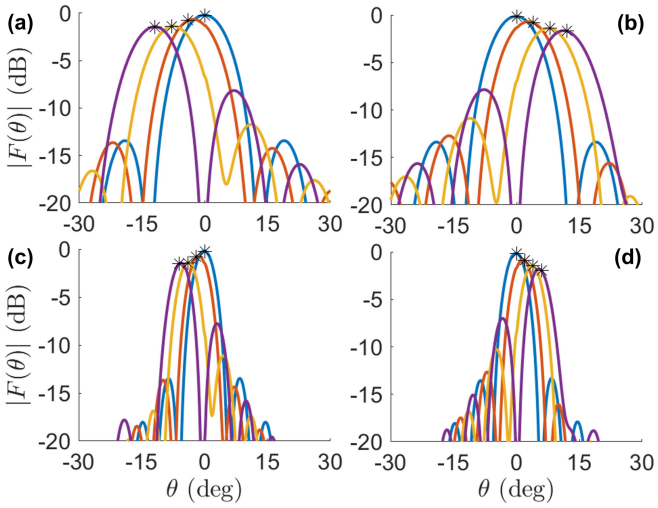


Fig. 21: Normalized radiation patterns at $f_\mathrm{c} = 2.45$ GHz for the wave-controlled RIS, obtained by optimizing W_b and f_b to maximize the radiated power at the angles marked by an asterisk; (a) and (b) correspond respectively to short- and open-circuit BTL terminations, with 27 RIS elements, with $\theta_\mathrm{p} = 0°, \pm4°, \pm8°$, and $\pm12°$; (c) and (d) correspond to short- and open-circuited BTLs, with 60 RIS elements, with with $\theta_\mathrm{p} = 0°, \pm2°, \pm4°$, and $\pm6°$.

C. Single Beam Control for Large Angles

For the wave-controlled RIS with a single biasing frequency, significant side lobes are created which limit the effectiveness of single beam-steering when the required phase range exceeds 360°. However, extending the application of this single-frequency methodology to these larger angles could be useful in applications where lower directivity and large side lobes are acceptable. To study this case, we apply a method for optimizing f_b and analyze the resulting radiation patterns.

To simplify the optimization of f_b, the conditions under which the BSW's phase gradient approximates the slope of the ideal phase gradient are found. This occurs when $\lambda_\alpha = \lambda_\mathrm{b}/4$, where λ_α is the spatial period of the ideal wrapped phase gradient. The spatial period is defined as $\lambda_\alpha = |x_{m_1} - x_{m_2}|$, where $x_{m_{1,2}}$ are positions along the BTL with reflected phases $\alpha_{m_{1,2}}$ such that $|\alpha_{m_1} - \alpha_{m_2}| = 2\pi$. Using (12), we find $\lambda_\alpha = \lambda_\mathrm{c}/|\sin(\theta_\mathrm{p})|$. This yields the following relationship between a given biasing frequency and the beam steering angle:

$$f_\mathrm{b} = \frac{f_\mathrm{c}\,|\sin(\theta_\mathrm{p})|}{4n_\mathrm{slow}}. \tag{13}$$

Several cases of radiation patterns using four biasing frequencies that are multiples of $f_{\mathrm{b},0}$ are shown in Fig. 22, each leading to different peak-radiation angles. These radiation patterns illustrate the limitations of the technique discussed in this section. The blue line corresponds to the limit of the near-broadside beam steering when $|\alpha_{M-1} - \alpha_0| = 360°$. The orange and purple lines correspond to biasing frequencies that create symmetric standing wave voltages around the center of the BTL ($w(m) = w(M-1-m)$) in (4)) and thus symmetric beam-splitting radiation patterns around $\theta = 0°$. The line in yellow shows that, when the standing-wave voltage is not symmetric and $|\alpha_{M-1} - \alpha_0| > 360°$, the radiation pattern has large sidelobes that reduce the directivity towards θ_p. This figure also compares the radiation patterns for the current design, shown in Fig. 22(a), to those of a lossless design with unit

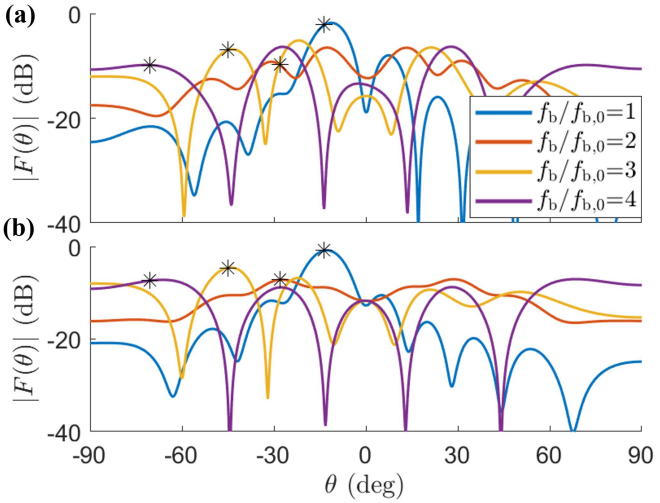


Fig. 22: Normalized radiation patterns for the short-circuited wave-controlled RIS operating at $f_c = 2.45$ GHz for four biasing frequencies that maximize reflection at the marked angles found from (13). The θ_p angles are $13.6°, 28.1°, 44.9°$, and $70.4°$. The results are presented for two cases: (a) the designed RIS board; (b) an ideal and lossless RIS with elements that have a perfectly linear phase-vs-voltage relationship.

cells that have a linear voltage-to-phase relationship for the carrier signal f_c, shown in Fig. 22(b). The linear relationship is calculated by $\alpha_m = 360° * (V - V_{\min}))/(V_{\max} - V_{\min})$, where V is the voltage applied to the unit cell, and $V_{\min} = 4$ and $V_{\max} = 15$ are the respective minimum and maximum voltages allowed for the design. These results illustrate that the beam steering method can be improved by using wider bandwidth elements [32].

An alternative approach for beam steering at large angles that uses the same optimization methods is to split the RIS into several segments with distinct BSWs. This method comes with certain trade-offs [30], but it avoids the creation of undesirable symmetric beams around $\theta = 0°$. Additionally, the beam steering angle can be extended using multi-resonant unit cells with a phase variation limit larger than $360°$ [25].

VI. Conclusions

This paper has presented a proof-of-concept wave-controlled RIS and a unified analytical, circuit-electromagnetic, and experimental study of its single-BSW biasing chain. The results validate the spatial periodicity of the generated dc bias and show that generator-BTL matching, distributed nonlinear rectifier loading, and nonideal peak detection determine the available control-voltage range. Matching Z_0 to Z_g makes both even and odd harmonics usable at the same ideal amplitude, whereas an unmatched source favors the odd harmonics. Additionally, this work demonstrates the feasibility of achieving reflective control of the RIS using a single standing-wave frequency, paving the way for more efficient and cost-effective implementations of dynamically reconfigurable metasurfaces.

The present hardware is not a performance limit of the concept. In particular, the peak detector, BTL geometry, matching network, and RIS unit cell represent design choices that can be jointly optimized to reduce loading and ripple, accelerate reconfiguration, and extend the dynamic phase range. Future work will directly measure reflected patterns with computer-controlled BTL excitation and Tx/Rx antennas connected to a network analyzer, and will quantify coupling under nonuniform bias using neighbor-perturbation measurements. Finally, the present work can be extended to two-dimensional control, which could be enabled using independently driven rows or orthogonal BTLs with multiple BSW harmonics.

Acknowledgment

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Appendix A
Derivation of the Analytical Model of the RIS Unit Cell

The realistic RIS circuit model shown in Fig. 3 is used to evaluate the reflection coefficient of the RIS [3], [20]. The equivalent impedance of the RIS, Z_{eq}, seen at the surface level by a normally incident plane wave, assuming that the varactor is not yet connected, is given by

$$Z_{eq} = \left(R_d + j\omega L_d + \frac{1}{j\omega C_d}\right) || \, j\omega L_s. \tag{14}$$

After some algebraic manipulations, we have

$$Z_{eq} = \frac{j\omega L_s \left(1 + j\omega R_d C_d - \omega^2 \left(L_d C_d\right)\right)}{1 + j\omega R_d C_d - \omega^2 C_d (L_d + L_s)}. \tag{15}$$

This expression can be reformulated in terms of the so-called electric resonance ω_e and magnetic resonance ω_m. At ω_e, the reflection phase is nearly $180°$, while near (but not exactly at) ω_m, the reflection phase is approximately $0°$. The magnetic resonance also plays a key role in manipulating the phase of the reflection coefficient and enabling its tunability [33]–[35]. These two resonances are defined as

$$\omega_e^2 = \frac{1}{C_d L_d}, \quad \omega_m^2 = \frac{1}{C_d \left(L_d + L_s\right)}, \tag{16}$$

leading to the final expression for the impedance at the surface of the RIS unit cell:

$$Z_{eq} = \frac{j\omega L_s \left(1 + j\omega R_d C_d - \left(\omega/\omega_e\right)^2\right)}{1 + j\omega R_d C_d - \left(\omega/\omega_m\right)^2}. \tag{17}$$

The numerical values for the circuit elements L_d, C_d, and R_d are determined by performing a single full-wave simulation of the RIS unit cell shown in Fig. 2 without including the varactor, the biasing via at the center of the patch, or the coplanar waveguide on the RIS board ground plane (it includes the via to GND and the small rectangular patch connected to it that will connect to the varactor). In our case, we use CST Studio Suite to model the RIS under an orthogonally incident plane wave polarized along y and traveling in the $-z$ direction, thereby accounting for mutual coupling among the RIS elements (we use periodic boundary conditions in x and y). The model also incorporates copper losses and relevant dielectric material properties. From this simulation, the scattering parameters are extracted, and the impedance Z_{eq}^{FW}

is computed from the Z-parameters to determine ω_e and ω_m. For simplicity, ω_e and ω_m are approximated by determining when the phase is exactly 180° and 0°, respectively. Then, the circuit element values are obtained as follows:

- The equivalent inductance L_s is analytically derived by modeling the dielectric substrate as a transmission line of length D in the z direction, with a ground plane termination. Using a Taylor series expansion, the impedance expression $j\omega L_s = j\sqrt{\mu_0/(\epsilon_0\epsilon_r)}\tan(\omega\sqrt{\epsilon_r}D/c)$ leads to the approximate value

$$L_s \approx \mu_0 D. \tag{18}$$

- Given L_s, the inductance L_d is obtained as

$$L_d = \frac{L_s}{(\omega_e/\omega_m)^2 - 1}. \tag{19}$$

- With L_d known, the capacitance C_d is determined using

$$C_d = \frac{1}{L_d\omega_e^2}. \tag{20}$$

- Finally, the resistance R_d is obtained from the real part of Z_{eq}^{FW} evaluated at ω_m in the full-wave simulation (at this frequency, the imaginary part is independent of R_d):

$$R_d = \frac{L_s}{C_d\,(1 + L_d/L_s)\,\Re\left(Z_{eq}^{FW}(\omega_m)\right)}. \tag{21}$$

Appendix B
Temporal Response Considerations

The temporal response is governed primarily by the rectifier, with $\tau_{dis} = R_rC_r$ and $\tau_{ch} \approx (R_{s,eq} + r_d)C_r$, where $R_{s,eq}$ and r_d are the effective source and diode dynamic resistances, respectively. Diode conduction near the positive crests produces an asymmetric nonlinear response: voltage rises through pulsed capacitor charging and falls mainly through R_rC_r discharge. Reducing R_r or C_r accelerates reconfiguration but increases ripple and charging current, whereas increasing R_rC_r improves voltage stability but slows the response.

Fig. 23 shows the measured steady-state rectifier voltages over the final 300 ns of the oscilloscope record for $2f_{b,0}$ and the final 100 ns for $5f_{b,0}$, both with a temporal resolution of 1 ns. The time axis is shifted so that $t = 0$ marks the beginning of each displayed interval. At $5f_{b,0}$, the peaks of $w_{pk,nr}(m)$, $w_{pk,r}(m)$, and $w(m)$, measured at $m = 26$, are 10.93, 10.47, and 9.07 V, respectively. At $2f_{b,0}$, measured at $m = 14$, they are 7.33, 6.8, and 6.47 V. At $2f_{b,0}$, $w_{pk,r}(m)$ is more susceptible to waveform distortion and measurement uncertainty. The measured ripple increases from $V_{r,pp} = 0.467$ V at $5f_{b,0}$ to 0.533 V at $2f_{b,0}$, consistent with the longer discharge interval at the lower frequency. According to Fig. 4a, near 9 V ($5f_{b,0}$ case), the ripple corresponds to a phase variation of approximately ±5°, while near 6.5 V ($2f_{b,0}$ case), the phase variation is approximately ±25°. The corresponding peak delays, approximately 3 ns at $5f_{b,0}$ and 2 ns at $2f_{b,0}$, are governed by the charging path, conduction interval, and waveform shape rather than by R_rC_r alone.

These measurements characterize steady-state rectifier operation; the total reconfiguration latency, including the combined

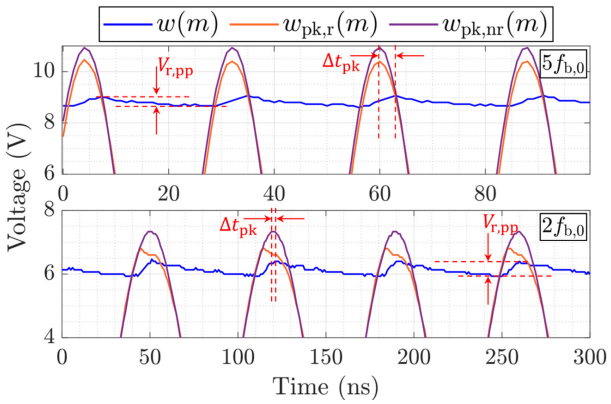

Fig. 23: Measured steady-state rectifier voltages at $2f_{b,0}$ and $5f_{b,0}$. Here, $V_{r,pp}$ is the output ripple and Δt_{pk} is the approximate delay between the peaks of $w_{pk,nr}(m)$ and $w(m)$. The input traces extend outside the acquisition range set by the 2 V/div scale and −6 V offset.

rectifier–varactor response, will be quantified from the rising and falling settling times in future work. A faster operation can be achieved by optimizing R_r and C_r, reducing the effective source impedance, employing diodes with lower junction capacitance and charge storage, or using active-envelope-detection or sample-and-hold architectures [19]. These alternatives must be evaluated together with their effects on ripple, loading, power consumption, and implementation complexity.

Appendix C
Maximization of W_b - Short-Circuit Termination

The amplitude W_b of the induced standing wave can be calculated as a function of the voltage V_{in} at the connection of the BTL with the signal generator:

$$W_b = \left|\frac{2V_{in}}{e^{-j\kappa} - e^{j\kappa}}\right|, \tag{22}$$

where $\kappa = (\omega_b n_{slow}/c)L_{tot}$. Assuming a BTL terminated in a short circuit, the input impedance of the BTL is $Z_{in} = jZ_0\tan(\kappa)$. Furthermore, assuming that at frequency f_b the capacitances C_f can be approximated as short circuits and the inductance L_f as an open circuit, we have

$$V_{in} = \frac{Z_{in}}{Z_{in} + Z_g}V_g = \frac{jZ_0\tan(\kappa)}{jZ_0\tan(\kappa) + Z_g}V_g. \tag{23}$$

The expression for W_b can thus be written as a function of the impedances Z_0 and Z_g:

$$W_b = \left|\frac{2\frac{jZ_0\tan(\kappa)}{jZ_0\tan(\kappa)+Z_g}V_g}{e^{-j\kappa} - e^{j\kappa}}\right|. \tag{24}$$

When considering the case with $f_b = nf_{b,0}$, the wavelength is $\lambda_b = 4L_{tot}/n$, resulting in $\kappa = n\pi/2$. When f_b is an odd multiple of $f_{b,0}$, we find that $\kappa = n\pi/2$, so $\tan(\kappa) = \infty$ and $e^{-j\kappa} - e^{j\kappa} = -j2$, leading to $W_b = V_g$, which as shown in Fig. 11 is always at its maximum value. However, when f_b is an even multiple of $f_{b,0}$, $\tan(\kappa) = 0$ while $e^{-j\kappa} - e^{j\kappa} = 0$, making it necessary to evaluate W_b in the limit as $\kappa \to n\pi/2$ for even n, leading to

$$W_b = \frac{Z_0}{Z_g}V_g. \tag{25}$$

This result indicates that when $Z_0 = Z_\mathrm{g}$, the amplitude of the standing wave equals V_g, the same value obtained when f_b is an odd multiple of $f_{\mathrm{b},0}$. In fact, under this matching condition, the specific value of κ becomes irrelevant. Indeed, evaluating (24) with $Z_0 = Z_\mathrm{g}$ gives

$$W_\mathrm{b}\Big|_{Z_0=Z_\mathrm{g}} = \left| \frac{2\frac{j\tan(\kappa)}{j\tan(\kappa)+1}V_\mathrm{g}}{e^{-j\kappa} - e^{j\kappa}} \right|. \tag{26}$$

This expression simplifies to

$$W_\mathrm{b}\Big|_{Z_0=Z_\mathrm{g}} = \left| \frac{-\tan(\kappa)}{j\sin(\kappa)\tan(\kappa) + \sin(\kappa)} V_\mathrm{g} \right| = V_\mathrm{g}. \tag{27}$$

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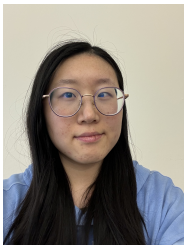

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