Power Management for Embedded Applications

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Presentation Flow

- Need for Power Management
- Basics of Power Consumption
- Static Power Reduction Techniques
- Dynamic Power Reduction Techniques

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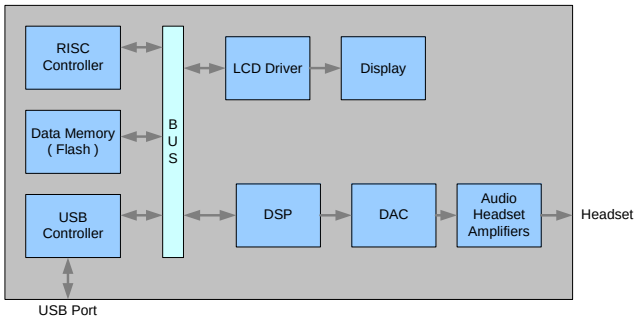
Need for Power Management

- Increasing Features & Complexity of Devices
- Battery Technology growth rate slower than the feature growth rate
  - Energy Capacity, Size & Cost
- Other Issues : Heat Dissipation

- Example:
  - Typical MP3 Player Li-ION Battery, for a Target Operation of 12 Hrs : 66 mA Max Power Consumption



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Need for Power Management

- Typical MP3 Player has (all values below are peaks):
  - System Controller : RISC Processor (@ 25 MHz) : 35mA to 50mA
  - DSP for Audio Processing : 16mA to 44mA (from table below)
  - Flash Memory and Memory Interface : 5ma to 10mA
  - USB Controller : 30mA to 55mA
  - Stereo DAC's and Headset Amps : 20mA to 25mA
  - LCD Interface : No Data. Very Wide Range.
  - Overall Total : 96mA to 184mA

Table 1 Representative Audio Decoder LSIs Aimed at Portable Players

Developer	Cirrus Logic, Inc (US)		Micronas Intermetall GmbH (Germany)	STMicroelectronics NV (Italy/France)	Texas Instruments, Inc (US)
Model	EP7209	Pending	MAS3507D	STA013	TSM320C6409
Decoding CPU	32-bit microcontroller (ARM720T, 74MHz)	24-bit fixed-point DSP	MP3 decoder*1	MP3 decoder	16-bit fixed-point DSP (100 MIPS)
Integrated interface, controller	Color LCD panel controller, IrDA interface, flash EEPROM interface, etc	1-bit ΔΣ DAC, 10-bit ADC for voice recording, SPDIF interface, etc	None	None	None
Supply voltage	+2.5V	+2.5V	+2.7 to +3.3V	+2.4 to +3.6V	+3.3V±10% *2
Dissipation	Max.110mW (f_s≥24kHz) Min.80mW (f_s≥24kHz)	Pending (under 40mW during MP3 decode)	Peak 85mW (at +2.7V)	Peak 90mW (at +2.4V)	Peak 60mW (at 80 MIPS)
Package	208-lead LQFP, 256-lead BGA	Pending	44-lead plastic LCC, 44-lead plastic QFP, 49-lead BGA	28-lead SOP, 44-lead TQFP	144-lead TQFP, 144-lead BGA (12-mm square footprint)
Price	LQFP US$11.95, BGA US$14.95 (unit price in lots of 100,000)	Pending	Pending	Pending	US$12.75 (unit price in lots of 10,000)
Shipment date	Sample shipping	Sample shipment in January 2000	Volume production in June 1999	Volume production in August 1999	Sample shipment in 3rd quarter 1999

*1Also supports ADPCM encode/decode *2Internal voltage +1.8V±10%

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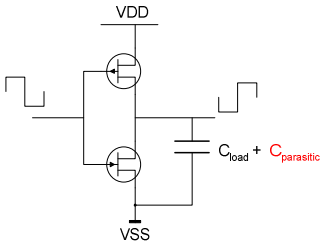
Basics of Power Consumption

- **Where is Power Consumed?**
  - **Static Power**
    - Leakage Paths in the Transistors
    - Higher as we go lower in the transistor size. At 0.25u this is negligible compared to the dynamic power.
    - Leakage scales at 1x, 3x, 10x, 40x, 110x, 400x for 0.25u, 0.18u, 130nm, 90nm, 65nm and 45 nm respectively
    - Varies over operating conditions (voltage, temperature etc) and is present even when no work is done.
  - **Dynamic Power**
    - Switching Nodes Consume Power
    - $P = C V^2 F$
    - Every Transition will consume power
    - Power Consumed when work is done
      - Usefulness of this work is not a factor



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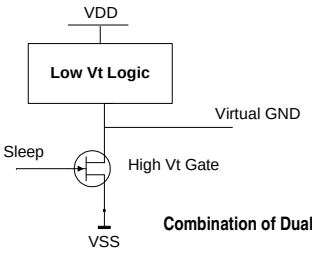
Static Power Reduction Techniques

- **Adaptive Body Biasing** – Reverse and Forward Biased Transistors : 2x to 4x Savings. Reverse used in Standby mode and No Bias/ Forward bias in active mode
- **Dual V_t Design :** Two Transistor with different V_t are used. Usage optimized based on the paths and the power consumption. Upto 10X savings
- **Sleep Transistors:** Virtual VDD & VSS planes created using logic. This is a very simple form on power gating. Upto 1000x power savings



Combination of Dual V_t and Sleep Transistor methods

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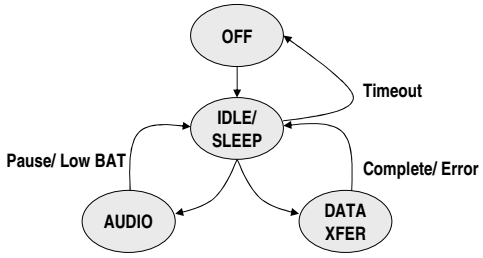
Dynamic Power Reduction Techniques

Device Performance/ Power Points

- **Device States:** This method classifies the operation of the devices into various modes and different techniques are associated with each mode for power savings (Overall Savings ranges from 20% to 60%). The possible states in the MP3 player are:



- **OFF :** Everything turned OFF. Device(s) Powered Down
- **IDLE/ SLEEP :** Device Powered Up. Controller which probably has an IDLE timer and the LCD logic are ON – everything Else is OFF.
- **AUDIO :** The DSP, DAC's and the LCD Logic are turned ON. USB controller is OFF. The Controller may be scaled down in frequency.
- **DATA XFER :** The DSP, DAC's are turned OFF. The USB controller is turned ON.

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Dynamic Power Reduction Techniques

- **ON :** This implies the the logic gets both power and clock. Performance could also traded OFF for power savings.

  - **Dynamic Frequency Scaling (DFS):** The frequency of the clock is reduced, thereby reducing the activity on the nets. During some operation modes, when it is not required to run some parts of the circuit at full speed, the clock frequency is dynamically altered by controlling the PLL / Clock Dividers. The voltage need not change. The relationship of DFS to Power Savings is almost linear.

  - **Dynamic Voltage Scaling (DVS):** The supply of the logic is lowered till a point where the logic is still functional for that technology. It might not operate at the desired frequency and hence DVS is most always associated with DFS (Dynamic frequency scaling). The relationship of DVS with Power Saving is Inverse-Square.

  - Intel SpeedStep™ is a combination of DVS and DFS. In this technology the software power manager detects the absence of an AC power supply and alters the voltage supply, the clock frequency of the core and the Bus Ratios.

  - AMD has slightly different power management scheme which runs the device at a lower performance levels even when the AC supply is present. The objective claimed is to maximize battery life and better thermal management.

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Dynamic Power Reduction Techniques

- **OFF :** The OFF logic has various definitions depending on the design:
  - Gated Clocks: Clocks are NOT present and hence no activity on the nets. The Power (supply) could be present.
  - Power Islands: These are independent subsystems operating on its power plane and clock. These allow flexibility for the power management entity to maximize savings by turning OFF entire subsystems when not in use.
  - Deep Sleep Mode: Used typically with memories – where the voltage of the memory is lowered to the retention voltage but the memory itself may not be operational at this point.
  - The Flip Side of the Power Islands & Deep Sleep modes are that it takes finite time to bring the subsystem back to operation, which depending on the operation might be a constraint.

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Dynamic Power Reduction Techniques

- **Scheduler Issues for Sleep/ Idle Mode**
  - Maximizing Sleep Mode duration minimizes power consumption. The trick is in determining optimal time to get into sleep mode.
    - Priority & Deadline of all the Pending tasks
    - Prevent short sleep modes by usage of statistical and known data. If we know that there will be an activity coming up shortly – its optimal to stay idle than goto sleep and wakeup.
    - Task Discarding – In the MP3 player, if the data buffer is not empty – the processing of this data can be delayed / discarded – based on sleep / time based power down if the user is paused / is powering down.
  - Getting out of Sleep mode is straight forward with the device waking up on an interrupt.
- IDLE mode consumes more power than sleep, but wakeup time is minimal

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Dynamic Power Reduction Techniques

StrongARM SA-1100			
State	**Performance**	**Hardware Latency**	**Electrical Power**
Sleep	Interrupts are detected and can awake the processor.	Entering sleep: 150 µs Exiting sleep: 10-157 ms	7.18 mW
Idle	No instructions are executed; interrupts put the processor in the run state.	Entering idle: < 10 cycles Exiting idle: < 10 cycles	55.5 mW at 59 MHz 81.9 mW at 133 MHz 95.5 mW at 192 MHz
Run	Performance is a function of processor frequency.	NA	Load Dependent

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Dynamic Power Reduction Techniques

- **Algorithm Selection & Switching**
  - Algorithm Selected has the biggest effect on the efficiency of the power management
  - Switching to a different computation algorithm.
    - Audio Quality can be traded off with the power consumption
    - Another example is the Half-Rate Vocoder in GSM Cell phones, that is used when the networks gets clogged – it is also used when the cell phone is low on battery.
- **Adaptive Scheduling:** Based on statistical data, scheduling mechanism altered.
  - Use of fixed scheduling rather than priority based helps in lowering power context switches. Cache usage also optimized.
- **Data Path Precision**: Most Embedded systems are data path intensive. Lowered precision / fixed precision on data path reduces overhead on the arithmetic engines & instruction scheduling.
- **Instruction Set Design**
- **Coding for Bus Transactions**
- **Feature Reduction**

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References

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Thank You!