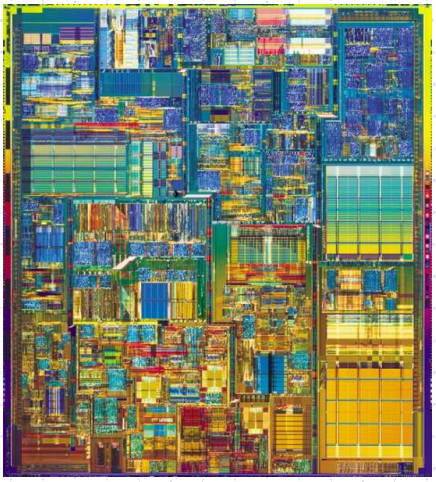
Target Processors



Layout of Intel P4 (Source: http://www.icknowledge.com/)

Kunal Deep Singh

EECS 298

November 5, 2004

Overview

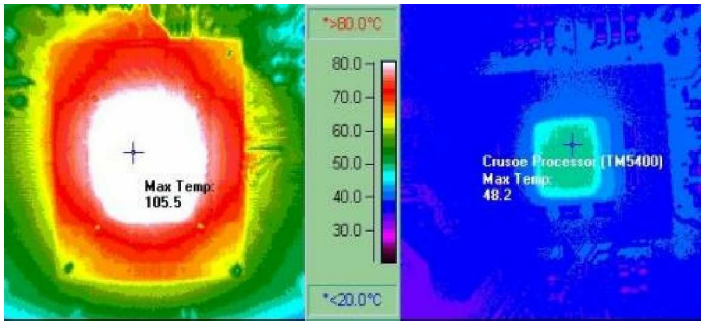
- Crusoe
- Power management
  - LongRun™
  - SpeedStep®
- StrongArm SA-1100
  - ARM & code reduction
  - ARM & Java
- ADSP- 219x DSP Processor
- DSP survey
- GPU survey (ATI and NVIDIA)
- Processor classification and branching
- Ultra-SPARC III Processor
- VLIW – in brief
- EPIC – in brief
- Microcontroller/Microprocessor survey

From Lecture

New ideas can actually reduce energy consumption

Pentium

Crusoe



Running the same multimedia application.

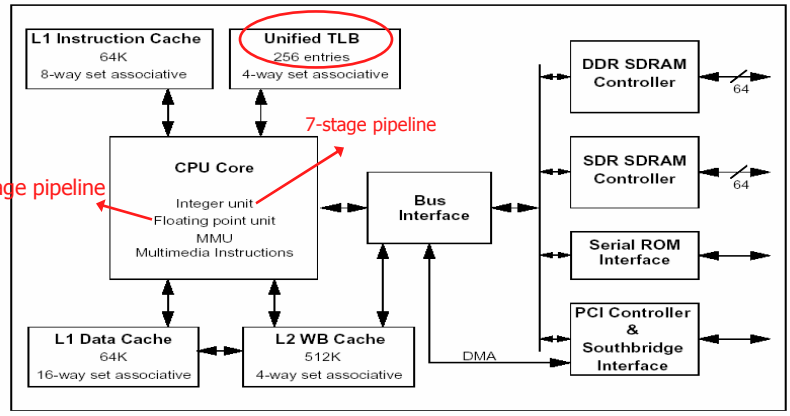
As published by Transmeta [www.transmeta.com]

Crusoe Processor Model TM5600/TM5400

- Multimedia applications
- VLIW processor - 128-bit instruction set
- 500-700 MHz
- Integrated 64K-byte L1 instruction cache, 64K-byte L1 data cache, and 512K-byte L2 write-back cache
- LongRun™ - power management
  - ultra-low power operation extends mobile battery life
  - 1-2 W @ 500-700 MHz, 1.2-1.6V running typical multimedia applications
  - 100 mW in deep sleep

TM5600 Architecture

For virtual memory mapping



Source: TM5600 Datasheet

TM5900 – the successor

Specifications	Crusoe TM5900 Processor
Frequency	800MHz - 1GHz
On-die L1 Instruction Cache	64 KB
On-die L1 Data Cache	64 KB
On-die L2 Write-Back Cache	512 KB
Integrated Northbridge Functionality	Yes
Integrated DDR Memory Controller	Supports DDR-266 SDRAM memory
Integrated PCI Interface	32-bit, 33MHz PCI
Full x86 Software and OS Compatibility	Yes
LongRun Power Management	Yes
LongRun Thermal Management	Yes
Package Type	Compact 399-contact FC-OBGA package
Package Size	21mm x 21mm
Manufacturing Process	0.13µm
Max. Thermal Design Power	As low as 6.5W - 9.5W (includes integrated northbridge)
Availability	Now

Source: TM5900 Product Brief

Crusoe™ SE Processor

- "To support a wide range of embedded applications, (these) processors are rated to run at full speed over the entire operating temperature range of 0ºC to 100ºC twenty four hours a day, seven days a week. Product life is rated to exceed 10 years while running at these performance and environmental extremes."

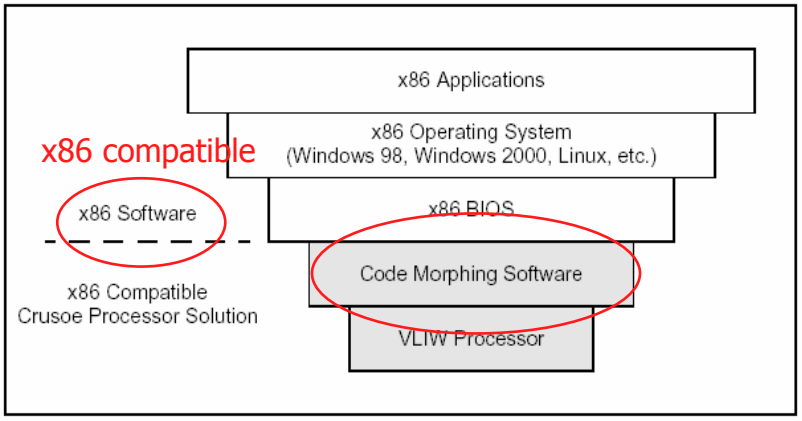
Transmeta Crusoe SE Processor Model TM55E	Transmeta Crusoe SE Processor Model TM58E
667 MHz	800 MHz - 933 MHz
128 KByte L1 Cache (64KByte L1 cache and 64 KByte L1 D-cache)	128 KByte L1 Cache (64KByte L1 cache and 64 KByte L1 D-cache)
256 KB L2 write-back cache	512 KB L2 write-back cache
Integrated Northbridge • 64-bit, 133 MHz DDR memory controller • 64-bit, 133 MHz SDR memory controller • 32-bit, 33 MHz, 3.3V PCI bus	Integrated Northbridge • 64-bit, 133 MHz DDR memory controller • 64-bit, 133 MHz SDR memory controller • 32-bit, 33 MHz, 3.3V PCI bus
MMX Instruction Support	MMX Instruction Support
0.13µm process	0.13µm process
Compact 474-pin Ceramic BGA Package	Compact 474-pin Ceramic BGA Package
Max TDP: 5.1 - 6.2W (includes Northbridge power)	Max TDP: 6.8 - 9.0W (includes Northbridge power)
Supports T-junction temperatures of 100C	Supports T-junction temperatures of 100C
Rated for 24/7 operation for 10 years	Rated for 24/7 operation for 10 years

Source: http://www.transmeta.com/crusoe/crusoe_se.html

LongRun™ - power management

- All Transmeta processor have this in common
- Power is proportional to the Vdd^2 and clock frequency
  - Hardware applies both DFS (Dynamic Frequency Scaling) and DVS (Dynamic Supply Voltage Scaling)
    - 32 levels of Vdd
    - PLL (phase lock loop) for scaling frequency between 500MHz and 700MHz in increments of 33MHz
  - Triggered by Software

TM5600 - Software Hierarchy



Source: TM5600 Datasheet

Code Morphing Software

- The translations from x86 are stored in a translation cache (part of main memory)
- Does instruction re-ordering, branch prediction, register renaming
- Well suited for the VLIW architecture – long instruction words allow for more information to be encoded per instruction
- All branching optimizations are done in software.
- Reduce power by reducing hardware
- More instructions to be executed
- The VLIW architecture – low performance degradation

Mobile Intel® Pentium® 4 Processors - M

- Used in Intel® Centrino™ mobile technology
- They use Intel® SpeedStep® Technology
  - Processor can switch between two core frequencies automatically based on CPU demand, without having to reset the processor or change the system bus frequency.
- 5 different states:
  - Normal State: This is the normal operating state for the processor.
  - AutoHALT: low-power state entered when the processor executes the HALT instruction.
  - Sleep state: low power state in which the processor maintains its context, maintains the phase-locked loop (PLL), and has stopped all internal clocks.
  - Deep Sleep state: very low power state the processor can enter while maintaining context. No transitions of signals are allowed on the system bus.
  - Deeper Sleep State: the lowest state power the processor can enter. This state is functionally identical to the Deep Sleep state but at a lower core voltage.

StrongARM® SA-1100

- The Intel® StrongARM® SA-1100 Microprocessor is the second member of the StrongARM® family.
- A highly integrated communications microcontroller that incorporates a 32-bit StrongARM® RISC processor core.
- Something interesting - the SA-1100 supports a 26-bit mode.
  - Reason: to avoid having an additional status register, earlier ARM processors used the top six bits of the program counter to hold status flags

Thumb Instruction Set

- ARM processors supported two instruction sets:
  - the ARM instruction set, 32-bits long, and
  - the Thumb instruction set instruction set which compresses the most-commonly used instructions into a 16-bit format.
- Thumb typically offers 30-40% code compression compared to ARM code.
  - Excellent code-density for minimal system memory size and cost
  - 32-bit performance from 8 or16-bit memory on an 8 or 16-bit bus for low system cost.
- On execution, these 16-bit instructions are decompressed transparently to full 32-bit ARM instructions in real time without performance loss.
- A standard ARM processor is fitted with a "Thumb decompressor" in the instruction pipeline.

ARM Jazelle® technology

- 32-bit embedded RISC architecture
- Java acceleration
- Jazelle technology adds a third instruction set - Java Byte Code - to the capability of the processor.
- Instruction set supports entering and exiting of Java applications, real-time interrupt handling, and debug support for mixed Java/ARM applications.
- The processor behaves like a Java machine. Once in Java state, the processor fetches and decodes Java byte codes and maintains the Java operand stack.

jazelle®
ARM® Acceleration Technology for the Java™ Platform

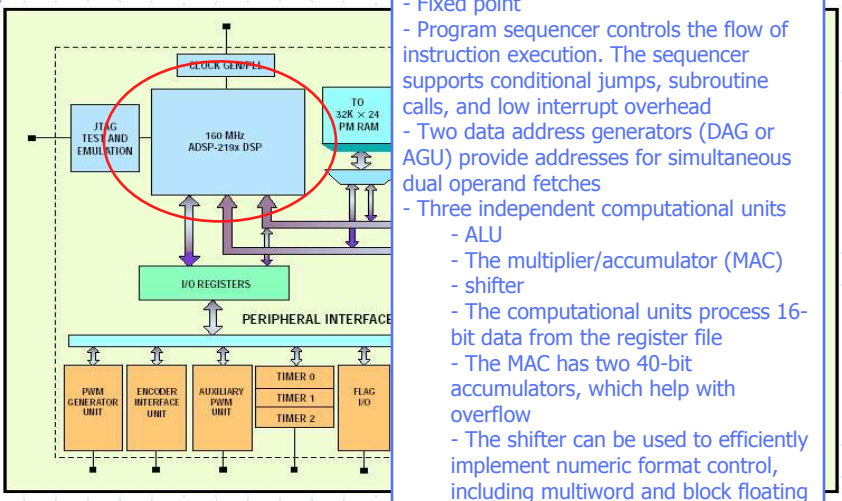
Source: http://www.arm.com/products/solutions/Jazelle.html

- Jazelle is completely compatible with the ARM interrupt and exception model - giving easy integration with Operating Systems and applications.
- mobile devices

ADSP- 219x DSP Processor

- 160 MHz, ADSP-219x DSP Core
- 8-Channel, 14-Bit, 20 MSPS ADC with On-Chip 1.0 Voltage Reference
- 40K Words of On-Chip RAM, Configured as 32K Words On-Chip 24-Bit Program RAM and 8K Words On-Chip 16-Bit Data RAM
- Incremental Encoder Interface Unit
- Three 32-Bit, General Purpose Timers
- 16-Bit General Purpose Flag I/O Port
- JTAG – for on board debugging
  - Capable of "pausing" the processor
  - Access the RAM modules
  - Access the internal registers
- Dedicated Memory DMA Controller for Data/Instruction
- Programmable PLL and Flexible Clock Generation
- Serial Peripheral Interface Communications Port with Master or Slave Operation
- Synchronous Serial Communications Port (SPORT)
- Integrated Watchdog Timer
- Dedicated Peripheral Interrupt Controller 17 interrupts based on a priority scheme

ADSP-219x



- 6.25 ns instruction cycle time
- Fixed point
- Program sequencer controls the flow of instruction execution. The sequencer supports conditional jumps, subroutine calls, and low interrupt overhead
- Two data address generators (DAG or AGU) provide addresses for simultaneous dual operand fetches
- Three independent computational units
  - ALU
  - The multiplier/accumulator (MAC)
  - shifter
  - The computational units process 16-bit data from the register file
  - The MAC has two 40-bit accumulators, which help with overflow
  - The shifter can be used to efficiently implement numeric format control, including multiword and block floating point representations.

DSP survey (Cores)

Licensor	Family	Floating, Fixed, or Both	Data Width	Instruction Width	Core Clock Speed [1]	Total Core Memory Space, Bytes	Core Voltage	Process	Notes
ARM	ARM7	Fixed point	32 bits	16/32 bits	133 MHz	4 G	1.2	0.13µm	Widely licensed 32-bit microprocessor core
	ARM9	Fixed point	32 bits	16/32 bits	250 MHz	4 G	1.2	0.13µm	Adds separate data bus for data access, deeper pipeline to ARM7
	ARM9E	Fixed point	16/32 bits	16/32 bits	250 MHz	4 G	1.2	0.13µm	ARM9 enhanced with single-cycle MAC unit
	ARM10E	Fixed point	16/32 bits	16/32 bits	325 MHz	4 G	1.2	0.13µm	Adds load/store unit, branch prediction, 64-bit buses
	ARM11	Fixed point	16/32 bits	16/32 bits	550 MHz	4 G	1.2	0.13µm	Adds SIMD and deeper pipeline
CEVA [9]	CEVA-TeakLite	Fixed point	16 bits	16 bits	190 MHz	256 K	1.2	0.13µm	Single-MAC, single-issue DSP core
	CEVA-Teak	Fixed point	16 bits	16 bits	180 MHz	8 M	1.2	0.13µm	Dual-MAC DSP core
	CEVA-Palm	Fixed point	16/20/24 bits	16/32 bits	180 MHz	32 M	1.2	0.13µm	Selectable data width, dual-MAC, dual-issue DSP core
	CEVA-X1620	Fixed point	8/16 bits	16/32 bits	450 MHz	4 G	1.2	0.13µm	8-way VLIW, dual-MAC DSP core
LSI Logic	ZSP200	Fixed point	16/32 bits	16 bits	260 MHz	256 K	1.2	0.13µm	2-way superscalar variant of the ZSP400
	ZSP400	Fixed point	16/32 bits	16 bits	260 MHz	256 K	1.2	0.13µm	4-way superscalar DSP core
	ZSP500	Fixed point	16/32 bits	16/32 bits	340 MHz	64 M	1.2	0.13µm	Second-generation ZSP; 4-way superscalar
	ZSP600	Fixed point	16/32 bits	16/32 bits	310 MHz	64 M	1.2	0.13µm	Second-generation ZSP; 6-way superscalar
Philips	CoolFlux	Fixed point	24 bits	32 bits	175 MHz	640 K	1.2	0.13µm	Dual-MAC core targets low-power audio applications
StarCore	SC1200	Fixed point	16 bits	16 bits	340 MHz	4 G	1.2	0.13µm	Dual-MAC, 4-issue variant of the SC1400
	SC1400	Fixed point	16 bits	16 bits	305 MHz	4 G	1.2	0.13µm	Synthesizable version of quad-MAC, 6-issue SC140
SuperH [11]	SH-4	Both	16/32 bits	16 bits	266 MHz	4 G	1.2	0.13µm	Superscalar microprocessor with 3D geometry instructions
	SH-5	Fixed point	16/32 bits	16/32 bits	400 MHz	4 G	1.2	0.13µm	Microprocessor with SIMD, optional floating-point
Tensilica	Xtensa LX/ Vectra LX	Fixed point	18 bits [12]	16/24/32/64 bits	370 MHz [13]	4 G	1.2	0.13µm	VLIW-based customizable core; compatible with Xtensa V

DSP survey (chips)

Vendor	Family	Floating, Fixed, or Both	Data Width	Instruction Width	Core Clock Speed [1]	Total On-Chip Memory, Bytes	Core Voltage	Notes
Agere Systems	DSP1641x	Fixed point	16 bits	16/32 bits	285 MHz	388 K–644 K	1.2, 1.575	Dual-MAC architecture
Analog Devices	ADSP-218x	Fixed point	16 bits	24 bits	80 MHz	20 K–256 K	1.8	Many family members w/ assorted peripherals
	ADSP-219x	Fixed point	16 bits	24 bits	160 MHz	20 K–160 K	2.5	Enhanced version of the ADSP-218x
	ADSP-2116x/ 2126x (SHARC)	Floating point	32/40 bits	48 bits	200 MHz	128 K–768 K	1.2, 1.8	Features SIMD, strong multiprocessor support
	ADSP-2136x (SHARC)	Floating point	32/40 bits	48 bits	333 MHz	896 K	1.2	SHARC with a lengthened pipeline for higher clock speeds
	ADSP-BF5xx (Blackfin)	Fixed point	16 bits	16/32 bits	750 MHz	84 K–328 K	0.8–1.45, 1.0–1.6	Dual-MAC DSP with variable speed and voltage
	ADSP-TS20x (TigerSHARC)	Both	8/16/32/ 40 bits	32 bits	600 MHz	512 K–3 M	1.0, 1.2	4-way VLIW with SIMD capabilities; uses eDRAM
Intel	PXA255/26x (XScale)	Fixed point	16/32 bits	16/32 bits	400 MHz	66 K–32 M	1.0–1.3	ARM-compatible; features SIMD support, "stacked" flash
	PXA27x (XScale/ Wireless MMX)	Fixed point	16/32 bits	16/32 bits	624 MHz	322 K–64 M	0.85–1.55	Adds 64-bit-wide SIMD operations and "stacked" SDRAM
LSI Logic	LSI40x (ZSP400)	Fixed point	16/32 bits	16 bits	200 MHz	96 K–252 K	1.2, 1.8	Based on ZSP400 licensable core (see below)
NEC	µPD77050 (SPX5)	Fixed point	16 bits	16/32 bits	250 MHz	400 K	0.9–1.5	Dual-MAC DSP with variable speed and voltage
Texas Instruments	TMS320C24x/ TMS320F24x	Fixed point	16 bits	16/32 bits	40 MHz	13 K–69 K	3.3	Hybrid microcontroller/DSP
	TMS320C28x/ TMS320F28x	Fixed point	32 bits	16/32 bits	150 MHz	40 K–294 K	1.8, 1.9	Hybrid microcontroller/DSP; assembly-compatible w/ 'C24x
	TMS320C54x	Fixed point	16 bits	16 bits	160 MHz	24 K–1280 K	1.5, 1.6, 1.8, 2.5	Many specialized instructions
	TMS320C55x	Fixed point	16 bits	8–48 bits	300 MHz	80 K–376 K	1.2–1.6, 1.26, 1.6	Dual-issue, dual-MAC DSP; assembly-compatible w/ 'C54x
	TMS320C62x	Fixed point	16 bits	32 bits	300 MHz	72 K–896 K	1.5, 1.8	8-way VLIW, dual-MAC DSP
	TMS320C64x	Fixed point	8/16 bits	32 bits	1 GHz	160 K–1056 K	1.1, 1.2, 1.4	Adds quad-MAC capabilities and specialized operations to 'C62x
	TMS320C67x	Floating point	32 bits	32 bits	300 MHz	72 K–264 K	1.2, 1.26, 1.4, 1.8, 1.9	Floating point version of 'C62x

ATI Chipset

Model Name	Core Clock (MHz)	RAM clock (MHz)	Pixel Pipeline	Texture Pipeline	Vertex Pipeline	RAM size (MB)	RAM Bus Width (bits)
X700 XT	500	1000	8	1	6	128/256	128
X800 SE	425	800	8	1	6	128/256	256
X800 Pro	475	900	12	1	6	256	256
X800 GT	425	900	16	1	6	256	256
X800 XT	500	1000	16	1	6	256	256
X800 XT PE	520	1120	16	1	6	256	256
9500	275	540	4	1	4	64/128	128
9500 Pro	275	540	8	1	4	128	128
9550	250	400	4	1	2	64/128/256	128
9550 SE	250	400	4	1	2	64/128/256	64
9600	325	400	4	1	2	128/256	128
9600 Pro	400	600	4	1	2	128/256	128
9600 SE	325	400	4	1	2	64/128/256	64
9600 XT	500	600	4	1	2	128/256	128
X300	325	400	4	1	2	64/128/256	128
X300 SE	325	400	4	1	2	64/128	64
X600 Pro	400	600	4	1	2	128/256	128
X600 XT	500	740	4	1	2	128/256	128
9700	275	540	8	1	4	128	256
9700 Pro	325	620	8	1	4	128	256
9800	325	600	8	1	4	128	256
9800 Pro	380	680	8	1	4	128/256	128
9800 Pro 128	380	680	8	1	4	128	256
9800 Pro 256	380	700	8	1	4	256	256
9800 SE 128	325	580	8	1	4	128	128
9800 SE 256	380	680	4	1	4	128	256
9800 XT	412	730	8	1	4	256	256

NVIDIA chipset

Model Name	Core Clock (MHz)	RAM clock (MHz)	Pixel Pipeline	Texture Pipeline	Vertex Pipeline	RAM size (MB)	RAM Bus Width (bits)
6600	300	550	8	1	3	128/256	128
6600GT	500	1000	8	1	3	128/256	128
6800LE	320	700	8	1	5	128	256
6800	325	700	12	1	5	128	256
6800GT	350	1000	16	1	6	256	256
6800U	400	1100	16	1	6	256	256
6800UE	450	1200	16	1	6	256	256
FX 5200LE	250	400	4	1	1	64/128	64
FX 5200	250	400	4	1	1	64/128/256	128
FX 5200U	325	650	4	1	1	128	128
FX 5500	270	400	4	1	1	128/256	128
FX5600XT	235	400	4	1	1	128/256	128
FX 5600	325	500	4	1	1	128/256	128
FX 5600U	350	700	4	1	1	128/256	128
FX 5600U FC	400	800	4	1	1	128	128
FX 5700LE	250	400	4	1	3	128/256	128
FX 5700	425	500	4	1	3	128/256	128
FX 5700U	475	900	4	1	3	128/256	128
FX 5700U GDDR3	475	950	4	1	3	128	128
FX 5800	400	800	4	2	2	128	128
FX 5800U	500	1000	4	2	2	128	128
FX 5900XT/SE	400	700	4	2	3	128	256
FX 5900	400	850	4	2	3	128/256	256
FX 5900U	450	850	4	2	3	256	256
FX 5950U	475	950	4	2	3	256	256

Processor classification and branching

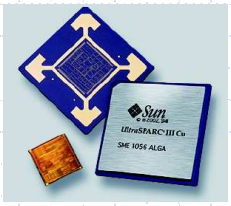
Name	Instruction	Pipeline	Instruction	Distinguishing Characteristic	Examples
Superscalar	Dynamic (by hardware)	Hardware	Static	In-order execution	Sun UltraSPARC II/III
Dynamic Superscalar	Dynamic (by hardware)	Hardware	Dynamic	Some out-of-order execution	IBM Power2
Speculative Superscalar	Dynamic (by hardware)	Hardware	Dynamic with speculation	Out-of-order execution	P III/4, MIPS R10K, Alpha 21264, HP PA 8500, IBM RS64III
VLIW	Static (by compiler)	Software	Static	No hazard	Trimedia, i860
EPIC	Mostly Static	Mostly software	Mostly Static	Explicit dependences marked by Compiler	Itanium

Multiple instructions fetched

- Branching - pipeline bubble – bottleneck
- Branch target buffers, branch local and global history (prediction) table – dynamic issue architectures
- Smart compilers – static issue architectures
- Alpha 21264 uses 29K bits of information to dynamically i.e. after branch instruction is fetched to predict branch taken or not taken
- SPEC95 benchmark – on average 99.4% accurate

Ultra-SPARC III Processor

- Used in Sun servers and workstations
- 64-bit open standards-based SPARC® V9 with VIS™ Instruction Set
- 4-way superscalar w/ 14-stage pipeline
- 16K-entry branch prediction table
- L1 cache: 64 KB 4-way Data, 32 KB 4-way Instruction, 2 KB Prefetch, 2 KB Write
- 4-GB memory subsystem per processor
  - Processor memory bandwidth scales with number of processors
- ALU: Six execution pipelines (2 integer, 2 FP/VIS, 1 load/store, 1 branch)



Source: UltraSPARC Family Brochure

- Sun unveils UltraSparc IV+ - Oct 5, 2004
- The UltraSparc IV+ 90-nanometer process technology clock speed of 1.8 - 2 GHz
- 2MB on-chip Level 2 cache, 32MB off-chip cache
- Two processor cores built onto the same chip
- By 2006 - Sparc64 VI processor, dual-core Sparc64 VI, 2.4 GHz, on-chip L2 cache of 6MB. Based on a 90-nm process technology.

VLIW – in brief

- The VLIW architecture is growing in popularity, particularly in the embedded market
- Multimedia and DSP
  - Philips's TriMedia
  - Chromatic's MPact Media Engine
  - Texas Instruments "VelociTI" C6X series of DSP
  - Various DSP by Analog Devices and StarCore (a joint venture of Motorola and Lucent)
- Unlike their superscalar opposites – VLIW processors do not spend a lot of time and silicon figuring out what to do and when to do it
- Result in elegant chip layout & hardware design takes a lot less time than for a superscalar processor
- The instruction-scheduling is performed by a trace-scheduling compiler

EPIC – in brief

- Superscalar processors must analyze code on the fly to determine the best execution path
- VLIW processors rely on their compiler - limited
- An EPIC processor relies on the compiler to explicitly arrange code to take advantage of parallelism
- Processor capable of processing lots of data in parallel
- EPIC processors have multiple instruction pipelines, many general-purpose registers, wide data paths, and also Predication and Speculation to aid them in keeping the code highly "pipelineable"
- Efficient combo
- An EPIC processor can use more of it's processing power to process meaningful operations
- Predication and speculation reduce branch mispredictions

Source: http://intel.com/go/itanium2

Microcontroller/Microprocessor survey - 8 bits

Company	Device	ISA	MHz	Inst. Width	V	Power (W)	DSP or MAC	FPU	Cache	MMU	Timers	Interrupts	ADC
Cypress	CY8C 22113	M8C	24	8, 16, 24	3 to 5.3	5mA	Yes				Up to 4 user defined 8/16/24 /32 bit	11	13-bit; 6/8-bit DAC
Dallas	DS80C 390/400	8051	40, 75	8	4.5 to 5.5	35 to 75 mA	Yes			Yes	3 or 4 16-bit + 1 watch dog	16	
Infineon	C868	8051	10	8	3.3	0.052	Yes				5 16-bit	9	4 channel 8-bit
NEC	K0/Kx1	NEC K	2 to 16	8	2.7 to 5.5	5 to 10 mA at 5V	Yes				8-bit, 16-bit, watch dog	NMI + 28 maskable	8 channel 8/10-bit
Philips	P89LP C92x	8051	12	8	2 to 4						4, real time	12, 3 external	4 channel 8-bit
ZiLOG	eZ80 F91	Z80/Z 180	50	8, 16, 24	3 to 3.6	230 mA			On-chip RAM or flash		4, watch dog	46	

Microcontroller/Microprocessor survey - 16 bits

Company	Device	ISA	MHz	Inst. Width	V	Power (W)	DSP or MAC	FPU	Cache	MMU	Timers	Interrupts	ADC
Freescale	HCS12 E series	HCS 12	25	16	3.3 to 5	0.325					3 16bit	20	16 channel 10-bit; 2 8-bit DAC
Intel	80C186 EC	x86	13, 16, 20, 25	8, 16	5 or 3	0.125		Co-processor			3 16bit		
Micro Chip	dsPIC	Modified Harvard	120	24	2.5 to 5.5		Yes				5 16bit	45	8 to 16 channel 12-bit
National Semi.	CP3BT 23		24	16	2.3 to 2.8	0.06	Yes				4 8bit	43	8 channel 12-bit
Renesas	M16C 6N	M16 C	20	16	4.2 to 5.5	0.7	Yes				11 16bit + 1 watch dof	9	26 channel 10-bit; 2 channel 8-bit DAC
TI	MSP 430 F147	MSP	8	16	1.8 to 2.6		Yes				16bit watch dog		8 channel 12-bit

Microcontroller/Microprocessor survey - 32 bits

Company	Device	ISA	MHz	Inst. Width	V	Power (W)	DSP or MAC	FPU	Cache	MMU	Timers	Interrupts	ADC
Analog Devices	ADuC 7027	ARM	45	16, 32	2.7 to 2.6	0.150	Yes				4 32bit	24	16 channel 12-bits
ARM	1176JZF-S	ARM V6Z	330 to 550	16, 32	1 to 1.2	0.5	Yes	Yes	4 to 64 KB	Yes	optional	Yes	optional
Freescale	ColdFire MCF523x	Cold Fire	80 to 150	16, 32, 48	1.5/ 3.3		Yes		8KB		4 32bit w/ DMA	Yes	
Fujitsu	FR60Lite	FR	33	16 (32bit bus)	3 to 5.5	0.250	Yes		4Kb inst		16-bit	24 external	8 or 16 channel 8/10bit; + 8bit DAC
Sharp	LH7A400	ARM	200	16,32	1.8/ 3.3	0.147	Yes		8KB inst and data	WinCE enabled	3 + 1 watch dog	24	
Xilinx	Power PC 405 in VirtexII PRO FPGA	Power PC	600	32	1 to 3.3	0.54	User defined DSP		16KB inst	Yes	Watch Dog	PowerPC capability	

Microcontroller/Microprocessor survey - 64 bits

Company	Device	ISA	MHz	Inst. Width	V	Power (W)	DSP or MAC	FPU	Cache	MMU	Timers	Interrupts
AMD	Mobile Athlon 64	x86	1600 to 2000	Variable	1.1 to 1.5	62		Yes	64/64 KB inst/data L2: 512KB			
MIPS	20Kc	MIPS64	600	64	1	1.5	Yes	Yes	32KB inst/data	Yes		
NEC	VR7701	MIPS64	400	64	1.5/ 2.5 or 2.2	4	Yes	Yes	32-KB inst/data two way	Yes	2 UART	6-bit addressing
PMC-Sierra	RM9150	MIPS64	600 to 1000	32	1.5, 2.5, 3.3	5 to 8	Yes	IEEE 754	16KB inst/data L2: 256KB 4 way set	Yes	4 + 1 watch dog	256 vectored
SuperH	SH5-103	SH compact	400	32/64	1.2	0.4	Yes	Yes + matrix and 3D vector	32KB inst/data 4 way set	Yes	3 + 1 watch dog + 1 real time	64
Toshiba	TMPR 4956CXB	MIPS64	350, 400, 450	64	1.2/ 3.3	0.7	Yes	Yes	32KB inst/data 2 way set	Yes		6 external


Thank You