

# ECE 298: System-on-Chip Description and Modeling Lecture 3

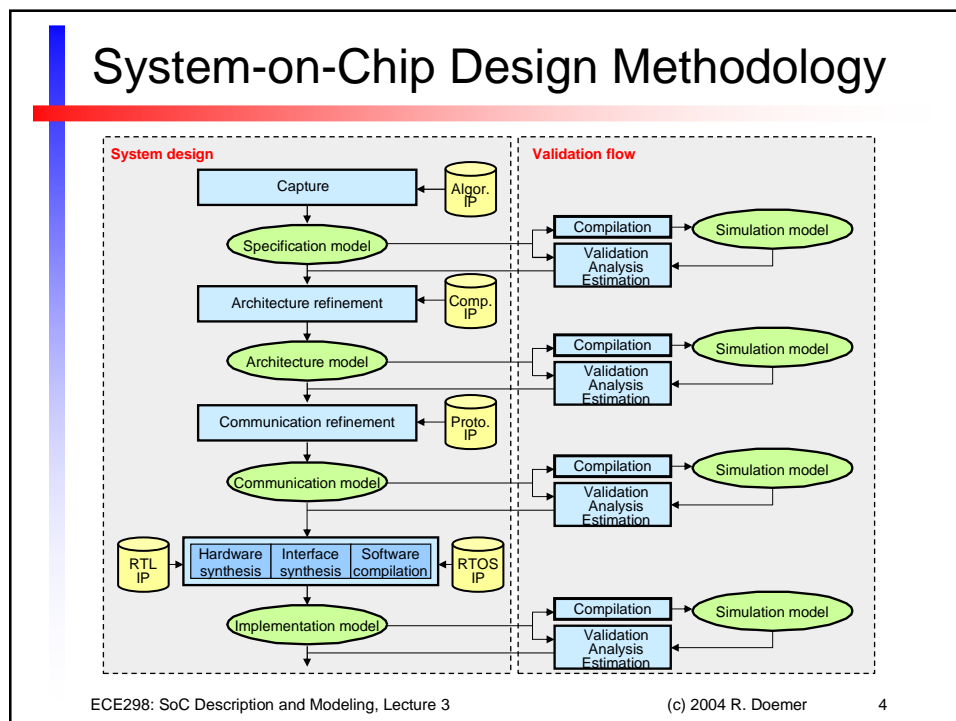
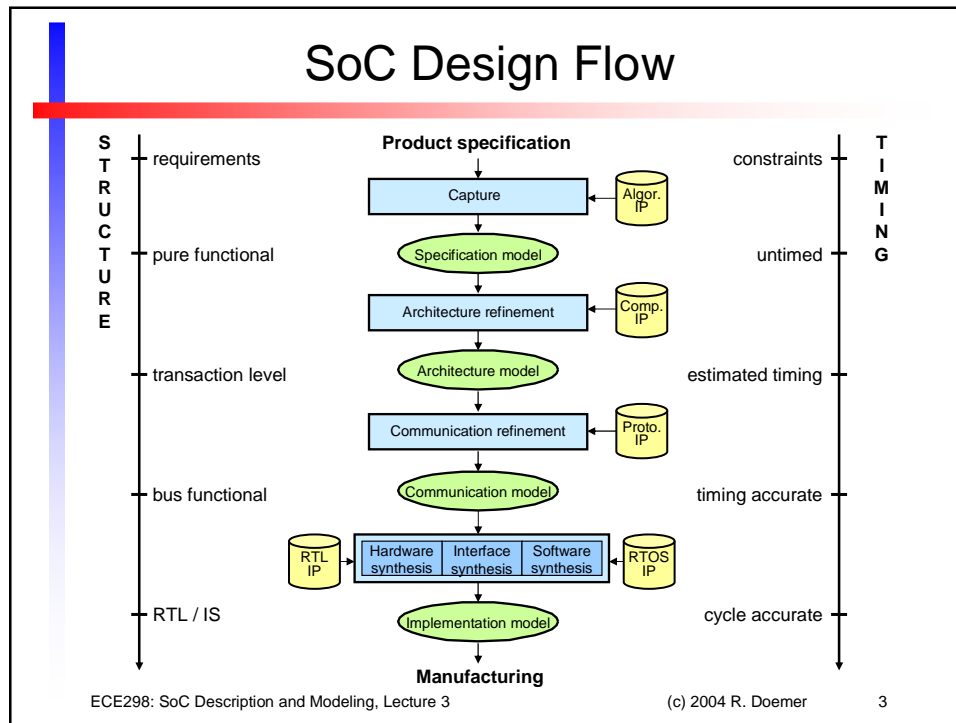
Rainer Dömer

doemer@uci.edu

The Henry Samueli School of Engineering  
Electrical Engineering and Computer Science  
University of California, Irvine

## Lecture 3: Overview

- SoC Design Methodology
- The SpecC Language
  - Foundation
  - Types
  - Structural and behavioral hierarchy
  - Concurrency
  - State transitions
  - Exception handling
  - Communication
  - Synchronization
  - Timing
  - RTL



## The SpecC Language

- Foundation: ANSI-C
  - Software requirements are fully covered
  - SpecC is a true superset of ANSI-C
  - Every C program is a SpecC program
  - Leverage of large set of existing programs
  - Well-known
  - Well-established

## The SpecC Language

- Foundation: ANSI-C
  - Software requirements are fully covered
  - SpecC is a true superset of ANSI-C
  - Every C program is a SpecC program
  - Leverage of large set of existing programs
  - Well-known
  - Well-established
- SpecC has extensions needed for hardware
  - Minimal, orthogonal set of concepts
  - Minimal, orthogonal set of constructs
- SpecC is a real language
  - Not just a class library

## The SpecC Language

- ANSI-C
  - Program is set of functions
  - Execution starts from function `main()`

```
/* HelloWorld.c */
#include <stdio.h>
void main(void)
{
    printf("Hello World!\n");
}
```

## The SpecC Language

- ANSI-C
  - Program is set of functions
  - Execution starts from function `main()`
- SpecC
  - Program is set of behaviors, channels, and interfaces
  - Execution starts from behavior `Main.main()`

```
/* HelloWorld.c */
#include <stdio.h>
void main(void)
{
    printf("Hello World!\n");
}
```

```
// HelloWorld.sc
#include <stdio.h>
behavior Main
{
    void main(void)
    {
        printf("Hello World!\n");
    }
};
```

## The SpecC Language

- SpecC types
  - Support for all ANSI-C types
    - predefined types (`int`, `float`, `double`, ...)
    - composite types (arrays, pointers)
    - user-defined types (`struct`, `union`, `enum`)
  - Boolean type: Explicit support of truth values
    - `bool b1 = true;`
    - `bool b2 = false;`
  - Bit vector type: Explicit support of bit vectors of arbitrary length
    - `bit[15:0] bv = 1111000011110000b;`
  - Event type: Support of synchronization
    - `event e;`
  - Buffered and signal types: Explicit support of RTL concepts
    - `buffered[clk] bit[32] reg;`
    - `signal bit[16] address;`

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9

## The SpecC Language

- Bit vector type
  - signed or unsigned
  - arbitrary length
  - standard operators
    - logical operations
    - arithmetic operations
    - comparison operations
    - type conversion
    - type promotion
  - concatenation operator
    - `a @ b`
  - slice operator
    - `a[l:r]`

```
typedef bit[7:0] byte; // type definition
byte          a;
unsigned bit[16] b;

bit[31:0] BitMagic(bit[4] c, bit[32] d)
{
    bit[31:0] r;

    a = 11001100b;           // constant
    b = 1111000011110000ub; // assignment

    b[7:0] = a;              // sliced access
    b = d[31:16];

    if (b[15])               // single bit
        b[15] = 0b;         // access

    r = a @ d[11:0] @ c      // concatenation
        @ 11110000b;

    a = ~(a & 11110000);    // logical op.
    r += 42 + 3*a;         // arithmetic op.

    return r;
}
```

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10

## The SpecC Language

- **buffered** type modifier
  - Representation of storage in RTL models
    - registers
    - register files
    - memories
    - etc.
  - Update at notification of specified events
    - synchronized with explicit clock

```

event Clk1, Clk2;           // system clock
buffered[Clk1] bit[32] R1;  // register
buffered[Clk1] bit[32] R2;

buffered[CLK2] bit[16] RF[64]; // register file
buffered[CLK2] bit[ 8] M[1024]; // memory

R1 = R2;           // swap contents of R1 and R2
R2 = R1;
wait CLK1;

RF[2] = RF[0] + RF[1];
...
wait CLK2;

```

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11

## The SpecC Language

- **signal** type modifier
  - Representation of wires and busses in RTL models
  - Semantics as in VHDL, Verilog

```

signal bit[31:0] addr; // address bus
signal bit[31:0] data; // data bus
buffered[CLK] M[1024];

wait addr;           // memory read access
data = M[addr];
...

wait addr && data;
M[addr] = data;     // memory write access
...

```

- Implemented as buffered variables with associated event

```

signal int x;   ⇔ buffered int x_v; event x_e;
x = 55;         ⇔ x_v = 55; notify x_e;
y = x + 2;     ⇔ y = x_v + 2;
wait x;        ⇔ wait x_e;
notify x;      ⇔ notify x_e;
wait (x == 5); ⇔ while(x_v != 5) { wait x_e; }

```

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12

## The SpecC Language

- Basic structure
  - Top behavior
  - Child behaviors
  - Channels
  - Interfaces
  - Variables (wires)
  - Ports

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## The SpecC Language

- Basic structure

```

interface I1
{
    bit[63:0] Read(void);
    void Write(bit[63:0]);
};

channel C1 implements I1;

behavior B1(in int, I1, out int);

behavior B(in int p1, out int p2)
{
    int v1;
    C1 c1;
    B1 b1(p1, c1, v1),
    b2(v1, c1, p2);

    void main(void)
    { par {
        b1;
        b2;
    }
};
    
```

SpecC 2.0:  
if *b* is a behavior instance,  
*b*; is equivalent to *b.main()*;

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## The SpecC Language

- Typical test bench
  - Top-level behavior: `Main`
  - Stimulator provides test vectors
  - Design unit under test
  - Monitor observes and checks outputs

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## The SpecC Language

- Behavioral hierarchy
 

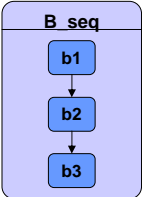
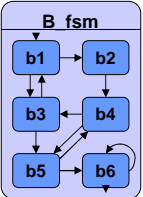
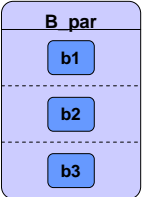
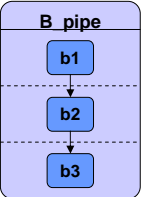
<p><b>Sequential execution</b></p> <pre style="background-color: #ffffcc; padding: 5px; font-family: monospace; font-size: small;"> behavior B_seq {   B b1, b2, b3;    void main(void)   {     b1;     b2;     b3;   } };                     </pre>	<p><b>FSM execution</b></p> <pre style="background-color: #ffffcc; padding: 5px; font-family: monospace; font-size: small;"> behavior B_fsm {   B b1, b2, b3,   b4, b5, b6;   void main(void)   {     fsm { b1:{...}           b2:{...}           ...}   } };                     </pre>	<p><b>Concurrent execution</b></p>	<p><b>Pipelined execution</b></p>
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## The SpecC Language

- Behavioral hierarchy

Sequential execution	FSM execution	Concurrent execution	Pipelined execution
			
<pre>behavior B_seq {   B b1, b2, b3;    void main(void)   {     b1;     b2;     b3;   } };</pre>	<pre>behavior B_fsm {   B b1, b2, b3,     b4, b5, b6;   void main(void)   {     fsm { b1:{...}           b2:{...}           ...}   } };</pre>	<pre>behavior B_par {   B b1, b2, b3;    void main(void)   {     par { b1;           b2;           b3; }   } };</pre>	<pre>behavior B_pipe {   B b1, b2, b3;    void main(void)   {     pipe { b1;            b2;            b3; }   } };</pre>

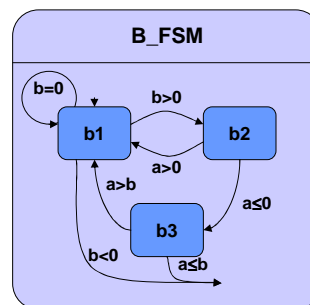
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17

## The SpecC Language

- Finite State Machine (FSM)
  - Explicit state transitions
    - triple  $\langle \text{current\_state}, \text{condition}, \text{next\_state} \rangle$
    - `fsm { <current_state> : { if <condition> goto <next_state> } ... }`
  - Moore-type FSM
  - Mealy-type FSM

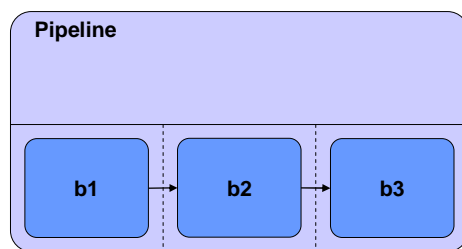
```
behavior B_FSM(in int a, in int b)
{
  B b1, b2, b3;

  void main(void)
  {
    fsm { b1: { if (b<0) break;
               if (b==0) goto b1;
               if (b>0) goto b2; }
          b2: { if (a>0) goto b1; }
          b3: { if (a>b) goto b1; }
        }
  }
};
```



## The SpecC Language

- Pipeline
  - Explicit execution in pipeline fashion
    - `pipe { <instance_list> };`



```
behavior Pipeline
{
    Stage1 b1;
    Stage2 b2;
    Stage3 b3;

    void main(void)
    {
        pipe
        { b1;
          b2;
          b3;
        }
    }
};
```

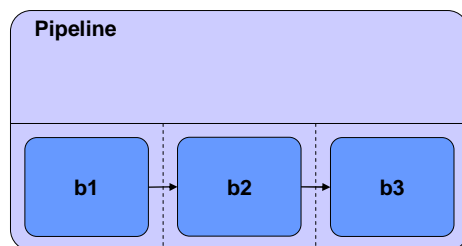
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19

## The SpecC Language

- Pipeline
  - Explicit execution in pipeline fashion
    - `pipe { <instance_list> };`
    - `pipe (<init>; <cond>; <incr>) { ... }`



```
behavior Pipeline
{
    Stage1 b1;
    Stage2 b2;
    Stage3 b3;

    void main(void)
    {
        int i;
        pipe(i=0; i<10; i++)
        { b1;
          b2;
          b3;
        }
    }
};
```

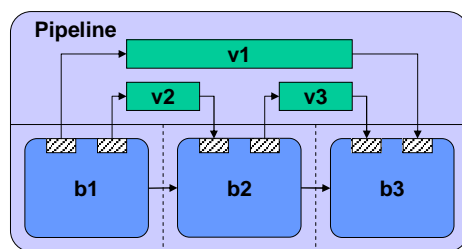
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20

## The SpecC Language

- Pipeline
  - Explicit execution in pipeline fashion
    - `pipe { <instance_list> };`
    - `pipe (<init>; <cond>; <incr>) { ... }`
  - Support for automatic buffering



```
behavior Pipeline
{
  int v1;
  int v2;
  int v3;

  Stage1 b1(v1, v2);
  Stage2 b2(v2, v3);
  Stage3 b3(v3, v1);

  void main(void)
  {
    int i;
    pipe(i=0; i<10; i++)
    {
      b1;
      b2;
      b3;
    }
  }
};
```

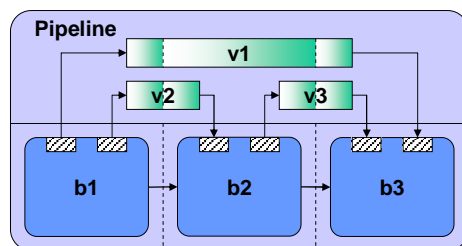
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21

## The SpecC Language

- Pipeline
  - Explicit execution in pipeline fashion
    - `pipe { <instance_list> };`
    - `pipe (<init>; <cond>; <incr>) { ... }`
  - Support for automatic buffering
    - `piped [...] <type> <variable_list>;`



```
behavior Pipeline
{
  piped piped int v1;
  piped int v2;
  piped int v3;

  Stage1 b1(v1, v2);
  Stage2 b2(v2, v3);
  Stage3 b3(v3, v1);

  void main(void)
  {
    int i;
    pipe(i=0; i<10; i++)
    {
      b1;
      b2;
      b3;
    }
  }
};
```

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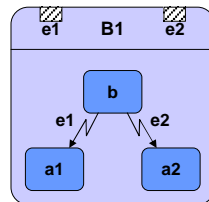
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22

## The SpecC Language

- Exception handling

- Abortion



```

behavior B1(in event e1, in event e2)
{
  B b, a1, a2;

  void main(void)
  { try { b; }
    trap (e1) { a1; }
    trap (e2) { a2; }
  };
};
  
```

- Interrupt

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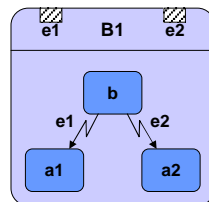
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23

## The SpecC Language

- Exception handling

- Abortion

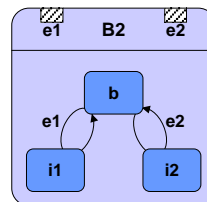


```

behavior B1(in event e1, in event e2)
{
  B b, a1, a2;

  void main(void)
  { try { b; }
    trap (e1) { a1; }
    trap (e2) { a2; }
  };
};
  
```

- Interrupt



```

behavior B2(in event e1, in event e2)
{
  B b, i1, i2;

  void main(void)
  { try { b; }
    interrupt (e1) { i1; }
    interrupt (e2) { i2; }
  };
};
  
```

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24

## The SpecC Language

---

- Communication
  - via shared variable

**Shared memory**

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25

## The SpecC Language

---

- Communication
  - via shared variable
  - via virtual channel

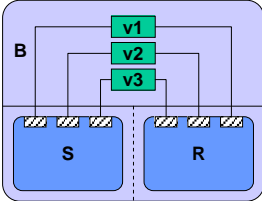
**Shared memory**

**Message passing**

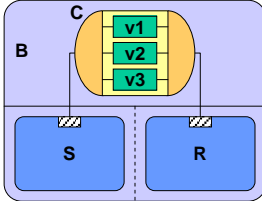
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26

## The SpecC Language

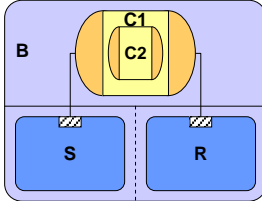
- Communication
  - via shared variable
  - via virtual channel
  - via hierarchical channel



Shared memory



Message passing

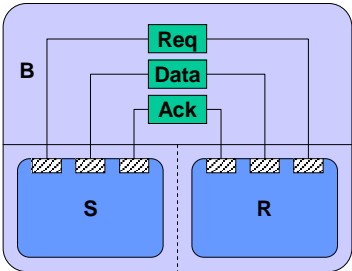


Protocol stack

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27

## The SpecC Language

- Synchronization
  - Event type
    - **event** <event\_List>;
  - Synchronization primitives
    - **wait** <event\_list>;
    - **notify** <event\_list>;
    - **notifyone** <event\_list>;



```

behavior S(out event Req,
           out float Data,
           in event Ack)
{
  float X;
  void main(void)
  {
    ...
    Data = X;
    notify Req;
    wait Ack;
    ...
  }
};

behavior R(in event Req,
           in float Data,
           out event Ack)
{
  float Y;
  void main(void)
  {
    ...
    wait Req;
    Y = Data;
    notify Ack;
    ...
  }
};
                    
```

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28

## The SpecC Language

- Communication
  - Interface class
    - **interface** <name> { <declarations> };
  - Channel class
    - **channel** <name> **implements** <interfaces> { <implementations> };

```

behavior S(IS Port)
{
    float X;
    void main(void)
    {
        ...
        Port.Send(X);
        ...
    }
};

behavior R(IR Port)
{
    float Y;
    void main(void)
    {
        ...
        Y=Port.Receive();
        ...
    }
};

interface IS
{
    void Send(float);
};

interface IR
{
    float Receive(void);
};

channel C
    implements IS, IR
{
    event Req;
    float Data;
    event Ack;

    void Send(float X)
    {
        Data = X;
        notify Req;
        wait Ack;
    }

    float Receive(void)
    {
        float Y;
        wait Req;
        Y = Data;
        notify Ack;
        return Y;
    }
};
                    
```

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## The SpecC Language

- Hierarchical channel
  - Virtual channel implemented by standard bus protocol
    - example: PCI bus

```

interface PCI_IF
{
    void Transfer(
        enum Mode,
        int NumBytes,
        int Address);
};

behavior S(IS Port)
{
    float X;
    void main(void)
    {
        ...
        Port.Send(X);
        ...
    }
};

behavior R(IR Port)
{
    float Y;
    void main(void)
    {
        ...
        Y=Port.Receive();
        ...
    }
};

interface IS
{
    void Send(float);
};

interface IR
{
    float Receive(void);
};

channel PCI
    implements PCI_IF;

channel C2
    implements IS, IR
{
    PCI Bus;
    void Send(float X)
    {
        Bus.Transfer(
            PCI_WRITE,
            sizeof(X), &X);
    }

    float Receive(void)
    {
        float Y;
        Bus.Transfer(
            PCI_READ,
            sizeof(Y), &Y);
        return Y;
    }
};
                    
```

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30

## The SpecC Language

- SpecC Standard Channel Library
  - introduced with SpecC Language Version 2.0
  - includes support for
    - mutex
    - semaphore
    - critical section
    - barrier
    - token
    - queue
    - handshake
    - double handshake
    - ...

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31

## The SpecC Language

- SpecC Standard Channel Library
  - mutex channel
  - semaphore channel

**c\_mutex**

**c\_semaphore**

```
interface i_semaphore
{
    void acquire(void);
    void release(void);
    void attempt(void);
};
```

```
channel c_mutex
implements i_semaphore;
```

```
channel c_semaphore(
    in const unsigned long c)
implements i_semaphore;
```

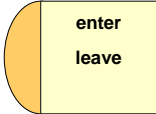
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32



## The SpecC Language

- SpecC Standard Channel Library
  - mutex channel
  - semaphore channel
  - critical section

**c\_critical\_section**



```

interface i_critical_section
{
    void enter(void);
    void leave(void);
};
                
```

↓

```

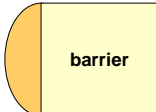
channel c_critical_section
implements i_critical_section;
                
```

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## The SpecC Language

- SpecC Standard Channel Library
  - mutex channel
  - semaphore channel
  - critical section
  - barrier

**c\_barrier**



```

interface i_barrier
{
    void barrier(void);
};
                
```

↓

```

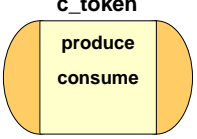
channel c_barrier(
    in unsigned long n)
implements i_barrier;
                
```

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## The SpecC Language

- SpecC Standard Channel Library
  - mutex channel
  - semaphore channel
  - critical section
  - barrier
  - token

```
interface i_token
{
  void consume(unsigned long n);
  void produce(unsigned long n);
};
```



**c\_token**

```
interface i_consumer
{
  void consume(unsigned long n);
};
```

```
interface i_producer
{
  void produce(unsigned long n);
};
```

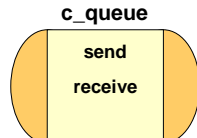
```
channel c_token
  implements i_consumer,
             i_producer,
             i_token;
```

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35

## The SpecC Language

- SpecC Standard Channel Library
  - mutex channel
  - semaphore channel
  - critical section
  - barrier
  - token
  - queue

```
interface i_tranceiver
{
  void receive(void *d, unsigned long l);
  void send(void *d, unsigned long l);
};
```



**c\_queue**

```
interface i_receiver
{
  void receive(void *d,
               unsigned long l);
};
```

```
interface i_sender
{
  void send(void *d,
            unsigned long l);
};
```

```
channel c_queue(
  in const unsigned long s)
  implements i_receiver,
             i_sender,
             i_tranceiver;
```

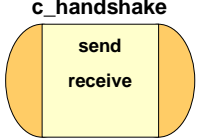
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36

## The SpecC Language

- SpecC Standard Channel Library
  - mutex channel
  - semaphore channel
  - critical section
  - barrier
  - token
  - queue
  - handshake

```
interface i_receive
{
  void receive(void);
};
```

```
interface i_send
{
  void send(void);
};
```



```
channel c_handshake
implements i_receive,
i_send;
```

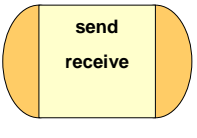
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37

## The SpecC Language

- SpecC Standard Channel Library
  - mutex channel
  - semaphore channel
  - critical section
  - barrier
  - token
  - queue
  - handshake
  - double handshake
  - ...

```
interface i_receiver
{
  void receive(void *d,
               unsigned long l);
};
```

```
interface i_sender
{
  void send(void *d,
            unsigned long l);
};
```



```
channel c_double_handshake
implements i_receiver,
i_sender;
```

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38

## The SpecC Language

- Timing
  - Exact timing
    - `waitfor <delay>;`

**Example: stimulator for a test bench**

```

behavior Testbench_Driver
(inout int a,
 inout int b,
 out event e1,
 out event e2)
{
  void main(void)
  {
    waitfor 5;
    a = 42;
    notify e1;

    waitfor 5;
    b = 1010b;
    notify e2;

    waitfor 10;
    a++;
    b |= 0101b;
    notify e1, e2;

    waitfor 10;
    b = 0;
    notify e2;
  }
};
    
```

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39

## The SpecC Language

- Timing
  - Exact timing
    - `waitfor <delay>;`
  - Timing constraints
    - `do { <actions> }`
    - `timing {<constraints>}`

**Example: SRAM read protocol**

```

Specification
bit[7:0] Read_SRAM(bit[15:0] a)
{
  bit[7:0] d;

  do { t1: {ABus = a; }
      t2: {RMode = 1;
           WMode = 0; }
      t3: { }
      t4: {d = Dbus; }
      t5: {ABus = 0; }
      t6: {RMode = 0;
           WMode = 0; }
      t7: { }
    }
  timing { range(t1; t2; 0; );
          range(t1; t3; 10; 20);
          range(t2; t3; 10; 20);
          range(t3; t4; 0; );
          range(t4; t5; 0; );
          range(t5; t7; 10; 20);
          range(t6; t7; 5; 10);
        }
  return(d);
}
    
```

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40

## The SpecC Language

- Timing
  - Exact timing
    - **waitfor** <delay>;
  - Timing constraints
    - **do** { <actions> }  
**timing** {<constraints>}

**Example: SRAM read protocol**

**Implementation 1**

```

bit[7:0] Read_SRAM(bit[15:0] a)
{
  bit[7:0] d;
  do { t1: {ABus = a; waitfor( 2);}
      t2: {RMode = 1;
           WMode = 0; waitfor(12);}
      t3: {
           waitfor( 5);}
      t4: {d = Dbus; waitfor( 5);}
      t5: {ABus = 0; waitfor( 2);}
      t6: {RMode = 0;
           WMode = 0; waitfor(10);}
      t7: { }
    }
  timing { range(t1; t2; 0; );
           range(t1; t3; 10; 20);
           range(t2; t3; 10; 20);
           range(t3; t4; 0; );
           range(t4; t5; 0; );
           range(t5; t7; 10; 20);
           range(t6; t7; 5; 10);
    }
  return(d);
}
                
```

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41

## The SpecC Language

- Timing
  - Exact timing
    - **waitfor** <delay>;
  - Timing constraints
    - **do** { <actions> }  
**timing** {<constraints>}

**Example: SRAM read protocol**

**Implementation 2**

```

bit[7:0] Read_SRAM(bit[15:0] a)
{
  bit[7:0] d; // ASAP Schedule
  do { t1: {ABus = a; }
      t2: {RMode = 1;
           WMode = 0; waitfor(10);}
      t3: {
           }
      t4: {d = Dbus; }
      t5: {ABus = 0; }
      t6: {RMode = 0;
           WMode = 0; waitfor(10);}
      t7: { }
    }
  timing { range(t1; t2; 0; );
           range(t1; t3; 10; 20);
           range(t2; t3; 10; 20);
           range(t3; t4; 0; );
           range(t4; t5; 0; );
           range(t5; t7; 10; 20);
           range(t6; t7; 5; 10);
    }
  return(d);
}
                
```

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42

## The SpecC Language

- RTL Modeling
  - Accellera RTL Semantics Standard
    - Style 1: *unmapped*
      - `a = b * c`
    - Style 2: *storage mapped*
      - `R1 = R1 * RF2[4]`
    - Style 3: *function mapped*
      - `R1 = ALU1(MULT, R1, RF2[4])`
    - Style 4: *connection mapped*
      - `Bus1=R1; Bus2=RF2[4]; Bus3=ALU1(MULT, Bus1, Bus2)`
    - Style 5: *exposed control*
      - `ALU_CTRL = 011001; RF2_CTRL = 010; ...`
  - Types specific for RTL:
    - `buffered` type modifier: Storage
    - `signal` type modifier: Communication
  - Control flow specific for RTL:
    - `fsm` construct: Explicit finite state machine with datapath

Source: <http://www.eda.org/alc-cwg/cwg-open.pdf>

## The SpecC Language

- RTL Modeling
  - `fsm` construct
    - Similar to `fsm` construct, but specifically for RTL
    - Explicit states and state transitions
    - State actions represent well-defined register transfers
      - limited to conditional/unconditional assignments and function calls
      - general loops, exceptions, synchronization, timing are not allowed
    - Explicit clock specifier
      - event list (external clock)
      - time delay (internal clock)
    - Explicit sensitivity list
      - needed for Mealy machine support
    - Explicit reset state
      - synchronous reset
      - asynchronous reset

## The SpecC Language

RTL  
Modeling  
Example

```
behavior FSMD_Example(
  signal in bool      CLK,          // system clock
  signal in bool      RST,          // system reset
  signal in bit[31:0] Inport,       // input ports
  signal in bit[1]    Start,        // input ports
  signal out bit[31:0] Outport,      // output ports
  signal out bit[1]    Done)
{
  void main(void)
  {
    fsmd(CLK)                      // clock + sensitivity
    {
      bit[32] a, b, c, d, e;        // local variables

      { Outport = 0;                // default
        Done = 0b;                  // assignments
      }

      if (RST) { goto S0;           // reset actions
      }

      S0 : { if (Start) goto S1;
            else      goto S0;
          }

      S1 : { a = b + c;              // state actions
            d = Inport * e;         // (register transfers)
            Outport = a;
            goto S2;
          }

      ... }
    }
  };
};
```

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45

## The SpecC Language

RTL  
Modeling  
Example

```
behavior FSMD_Example(
  signal in bool      CLK,          // system clock
  signal in bool      RST,          // system reset
  signal in bit[31:0] Inport,       // input ports
  signal in bit[1]    Start,        // input ports
  signal out bit[31:0] Outport,      // output ports
  signal out bit[1]    Done)
{
  void main(void)
  {
    fsmd(CLK)                      // clock + sensitivity
    {
      bit[32] a, b, c, d, e;        // local variables

      { Outport = 0;                // default
        Done = 0b;                  // assignments
      }

      if (RST) { goto S0;           // reset actions
      }

      S0 : { if (Start) goto S1;
            else      goto S0;
          }

      S1 : { a = b + c;              // state actions
            d = Inport * e;         // (register transfers)
            Outport = a;
            goto S2;
          }

      ... }
    }
  };
};
```

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46

## The SpecC Language

RTL  
Modeling  
Example

```
behavior FSMD_Example(
  signal in bool    CLK,          // system clock
  signal in bool    RST,          // system reset
  signal in bit[31:0] Inport,     // input ports
  signal in bit[1]  Start,        //
  signal out bit[31:0] Outport,   // output ports
  signal out bit[1]  Done)
{
  void main(void)
  {
    fsmd(CLK; Inport, Start)      // clock + sensitivity
    {
      bit[32] a, b, c, d, e;      // local variables

      { Outport = 0;              // default
        Done = 0b;                // assignments
      }

      if (RST) { goto S0;         // reset actions
      }

      S0 : { if (Start) goto S1;
            else goto S0;
          }

      S1 : { a = b + c;           // state actions
            d = Inport * e;      // (register transfers)
            Outport = a;
            goto S2;
          }

      ... }
    }
};
```

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47

## The SpecC Language

RTL  
Modeling  
Example

```
behavior FSMD_Example(
  signal in bool    CLK,          // system clock
  signal in bool    RST,          // system reset
  signal in bit[31:0] Inport,     // input ports
  signal in bit[1]  Start,        //
  signal out bit[31:0] Outport,   // output ports
  signal out bit[1]  Done)
{
  void main(void)
  {
    fsmd(CLK; RST)               // asynchronous reset
    {
      bit[32] a, b, c, d, e;      // local variables

      { Outport = 0;              // default
        Done = 0b;                // assignments
      }

      if (RST) { goto S0;         // reset actions
      }

      S0 : { if (Start) goto S1;
            else goto S0;
          }

      S1 : { a = b + c;           // state actions
            d = Inport * e;      // (register transfers)
            Outport = a;
            goto S2;
          }

      ... }
    }
};
```

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48



## The SpecC Language

RTL  
Modeling  
Example

```
behavior FSMD_Example(
  signal in bool    CLK,           // system clock
  signal in bool    RST,           // system reset
  signal in bit[31:0] Inport,      // input ports
  signal in bit[1]  Start,         //
  signal out bit[31:0] Outport,    // output ports
  signal out bit[1]  Done)
{
  void main(void)
  {
    fsmd(CLK)                       // clock + sensitivity
    {
      bit[32] a, b, c, d, e;        // local variables

      { Outport = 0;                // default
        Done = 0b;                  // assignments
      }

      if (RST) { goto S0;          // reset actions
      S0 :     { if (Start) goto S1;
                else      goto S0;
      S1 :     { a = b + c;         // state actions
                d = Inport * e;    // (register transfers)
                Outport = a;
                goto S2;
                ... }
    }
  };
};
```

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49

## The SpecC Language

RTL  
Modeling  
Example

```
behavior FSMD_Example(
  signal in bool    CLK,           // system clock
  signal in bool    RST,           // system reset
  signal in bit[31:0] Inport,      // input ports
  signal in bit[1]  Start,         //
  signal out bit[31:0] Outport,    // output ports
  signal out bit[1]  Done)
{
  void main(void)
  {
    fsmd(CLK)                       // clock + sensitivity
    {
      bit[32] a, b, c, d, e;        // local variables

      { Outport = 0;                // default
        Done = 0b;                  // assignments
      }

      if (RST) { goto S0;          // reset actions
      S0 :     { if (Start) goto S1;
                else      goto S0;
      S1 :     { a = b + c;         // state actions
                d = Inport * e;    // (register transfers)
                Outport = a;
                goto S2;
                ... }
    }
  };
};
```

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50

## The SpecC Language

RTL  
Modeling  
Example

```
behavior FSMD_Example(
  signal in bool    CLK,          // system clock
  signal in bool    RST,          // system reset
  signal in bit[31:0] Inport,     // input ports
  signal in bit[1]  Start,        //
  signal out bit[31:0] Outport,   // output ports
  signal out bit[1]  Done)
{
  void main(void)
  {
    fsmd(CLK)                      // clock + sensitivity
    {
      bit[32] a, b, c, d, e;       // local variables

      { Outport = 0;               // default
        Done = 0b;                // assignments
      }

      if (RST) { goto S0;         // reset actions
      }

      S0 : { if (Start) goto S1;
            else      goto S0;
          }

      S1 : { a = b + c;            // state actions
            d = Inport * e;       // (register transfers)
            Outport = a;
            goto S2;
          }

      ...
    }
  }
};
```

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51

## The SpecC Language

RTL  
Modeling  
Example

```
behavior FSMD_Example(
  signal in bool    CLK,          // system clock
  signal in bool    RST,          // system reset
  signal in bit[31:0] Inport,     // input ports
  signal in bit[1]  Start,        //
  signal out bit[31:0] Outport,   // output ports
  signal out bit[1]  Done)
{
  void main(void)
  {
    fsmd(CLK)                      // clock + sensitivity
    {
      bit[32] a, b, c, d, e;       // unmapped variables

      { Outport = 0;               // default
        Done = 0b;                // assignments
      }

      if (RST) { goto S0;         // reset actions
      }

      S0 : { if (Start) goto S1;
            else      goto S0;
          }

      S1 : { a = b + c;            // Accellera style 1
            d = Inport * e;       // (unmapped)
            Outport = a;
            goto S2;
          }

      ...
    }
  }
};
```

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52

## The SpecC Language

RTL  
Modeling  
Example

```
behavior FSMD_Example(
  signal in bool    CLK,          // system clock
  signal in bool    RST,          // system reset
  signal in bit[31:0] Inport,     // input ports
  signal in bit[1]  Start,        // Start
  signal out bit[31:0] Outport,   // output ports
  signal out bit[1]  Done)
{
  void main(void)
  {
    fsmd(CLK)                    // clock + sensitivity
    {
      buffered[CLK] bit[32] RF[4]; // register file
      {
        Outport = 0; // default
        Done = 0b; // assignments
      }
      if (RST) { goto S0; // reset actions
      }
      S0 : { if (Start) goto S1;
            else goto S0;
          }
      S1 : { RF[0]=RF[1]+RF[2]; // Accellera style 2
            RF[3]=Inport*RF[4]; // (storage mapped)
            Outport = RF[0];
            goto S2;
          }
      ...
    }
  }
};
```

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53

## The SpecC Language

RTL  
Modeling  
Example

```
behavior FSMD_Example(
  signal in bool    CLK,          // system clock
  signal in bool    RST,          // system reset
  signal in bit[31:0] Inport,     // input ports
  signal in bit[1]  Start,        // Start
  signal out bit[31:0] Outport,   // output ports
  signal out bit[1]  Done)
{
  void main(void)
  {
    fsmd(CLK)                    // clock + sensitivity
    {
      buffered[CLK] bit[32] RF[4]; // register file
      {
        Outport = 0; // default
        Done = 0b; // assignments
      }
      if (RST) { goto S0; // reset actions
      }
      S0 : { if (Start) goto S1;
            else goto S0;
          }
      S1 : { RF[0] = // Accellera style 3
            ADD0(RF[1],RF[2]); // (function mapped)
            RF[3] =
            MUL0(Inport,RF[4]);
            Outport = RF[0];
            goto S2;
          }
      ...
    }
  }
};
```

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54

## The SpecC Language

RTL  
Modeling  
Example

```
behavior FSMD_Example(
  signal in bool    CLK,           // system clock
  signal in bool    RST,           // system reset
  signal in bit[31:0] Inport,      // input ports
  signal in bit[1]  Start,         // Start,
  signal out bit[31:0] Outport,    // output ports
  signal out bit[1]  Done)
{
  void main(void)
  {
    fsmd(CLK)                       // clock + sensitivity
    {
      buffered[CLK] bit[32] RF[4];   // register file
      bit[32] BUS0, BUS1, BUS2;     // busses
      {
        Outport = 0;               // default
        Done = 0b;                 // assignments
      }

      if (RST) { goto S0;           // reset actions
    }

    S0 : {
      if (Start) goto S1;
      else       goto S0;
    }

    S1 : {
      BUS0 = RF[1];                // Accellera style 4
      BUS1 = RF[2];                // (connection mapped)
      BUS3 = ADD0(BUS0,BUS1);
      RF[0]= BUS3;
      ...
      goto S2;
    }
  }
};
```

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55

## The SpecC Language

RTL  
Modeling  
Example

```
behavior FSMD_Example(
  signal in bool    CLK,           // system clock
  signal in bool    RST,           // system reset
  signal in bit[31:0] Inport,      // input ports
  signal in bit[1]  Start,         // Start,
  signal out bit[31:0] Outport,    // output ports
  signal out bit[1]  Done)
{
  void main(void)
  {
    fsmd(CLK)                       // clock + sensitivity
    {
      signal bit[5:0] RF_CTRL;      // control wires
      signal bit[1:0] ADD0_CTRL, MUL0_CTRL;
      {
        Outport = 0;               // default
        Done = 0b;                 // assignments
      }

      if (RST) { goto S0;           // reset actions
    }

    S0 : {
      if (Start) goto S1;
      else       goto S0;
    }

    S1 : {
      RF_CTRL = 011000b;           // Accellera style 5
      ADD0_CTRL = 01b;            // (exposed control)
      MUL0_CTRL = 11b;
      ...
      goto S2;
    }
  }
};
```

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56

## The SpecC Language

- Library support
  - Import of precompiled SpecC code
    - **import** <component\_name>;
  - Automatic handling of multiple inclusion
    - no need to use **#ifdef** - **#endif** around included files
  - Visible to the compiler/synthesizer
    - not inline-expanded by preprocessor
    - simplifies reuse of IP components

```
// MyDesign.sc  
  
#include <stdio.h>  
#include <stdlib.h>  
  
import "Interfaces/I1";  
import "Channels/PCI_Bus";  
import "Components/MPEG-2";  
  
...
```

## The SpecC Language

- Persistent annotation
  - Attachment of a key-value pair
    - globally to the design, i.e. **note** <key> = <value>;
    - locally to any symbol, i.e. **note** <symbol>.<key> = <value>;
  - Visible to the compiler/synthesizer
    - eliminates need for pragmas
    - allows easy data exchange among tools

## The SpecC Language

- Persistent annotation
  - Attachment of a key-value pair
    - globally to the design, i.e. **note** <key> = <value>;
    - locally to any symbol, i.e. **note** <symbol>.<key> = <value>;
  - Visible to the compiler/synthesizer
    - eliminates need for pragmas
    - allows easy data exchange among tools

SpecC 2.0:  
<value> can be a  
composite constant  
(just like complex  
variable initializers)

```

/* comment, not persistent */

// global annotations
note Author = "Rainer Doemer";
note Date   = "Fri Feb 23 23:59:59 PST 2001";

behavior CPU(in event CLK, in event RST, ...)
{
  // local annotations
  note MinMaxClockFreq = {750*1e6, 800*1e6 };
  note CLK.IsSystemClock = true;
  note RST.IsSystemReset = true;
  ...
};

```

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59

## Summary

- SpecC model
  - PSM model of computation
  - Separation of communication and computation
  - Hierarchical network of behaviors and channels
- SpecC language
  - True superset of ANSI-C
    - ANSI-C plus extensions for HW-design
  - Support of all concepts needed in system design
    - Structural and behavioral hierarchy
    - Concurrency
    - State transitions
    - Communication
    - Synchronization
    - Exception handling
    - Timing
    - RTL

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60