

# ECE 298: System-on-Chip Description and Modeling Lecture 4

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## Lecture 4: Overview

- Homework Assignment 1
  - Discussion and Solution
- System-on-Chip Specification
  - Essential Issues
  - SoC Specification
  - Specification Model
  - Specification Language
  - Specification Modeling Guidelines
  - Specification Example
- System-on-Chip Environment (SCE)
  - Demonstration
- Homework Assignment 2
  - Administration
  - Tasks

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## Homework Assignment 1

- Discussion and Solution
  - Task 1: Get familiar with MPEG-Audio
    - MPEG = Moving Picture Experts Group
    - Coding of audio-visual information in digital streams
    - High compression ratio (lossy compression)
    - MPEG Audio
      - 3 layers (layer 3 is also known as MP3)
      - Decoded data: stream of samples, e.g. at 44.1kHz
      - Encoded data: frames of N samples, compressed to stream of 32 to 448 kbit/sec
  - Task 2: Install *mpg123* package
    - Online demo
  - Task 3: Find an example and try the software
    - Online demo (source: <ftp://ftp.fhg.de/pub/layer3>)

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## Homework Assignment 1

- Discussion and Solution
  - Task 4: Get familiar with the implementation
    - How many source files? • 56 tool, 10 lib (.c and .h)
    - Dependency of source files? • see Makefile!
    - How many lines of code?
      - Total? – 15235 tool, 3623 lib
      - Testbench? – 15235 – 3623 = 11612
      - Encoder? – 0
      - Decoder? – 3623
    - How many functions? • 30
    - Calling tree of the functions? • Use RedHat **snavigator**
    - What kind of operations? • =, \*, -, [], etc.
    - Any special considerations regarding implementation? • decoding tables (cos(), etc.) can be hardwired in ROM

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## Specification Issues

- An Example ...

Proposed by the project team
Product specification
Product design by senior analyst

Product after implementation
Product after acceptance by user
What the user wanted

*Source: unknown author*

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## SoC Specification

**Specification Capture and Validation**

```

    graph TD
        subgraph Capture_Validation [Specification Capture and Validation]
            Capture[Capture] --> SpecModel([Specification model])
            AlgorIP[(Algor. IP)] --> SpecModel
            SpecModel --> Comp1[Compilation]
            SpecModel --> Val1[Validation Analysis Estimation]
            Comp1 --> Sim1([Simulation model])
            Val1 --> Sim1
        end

        SpecModel --> ArchRef[Architecture refinement]
        CompIP[(Comp. IP)] --> ArchRef
        ArchRef --> ArchModel([Architecture model])
        ArchModel --> Comp2[Compilation]
        ArchModel --> Val2[Validation Analysis Estimation]
        Comp2 --> Sim2([Simulation model])
        Val2 --> Sim2

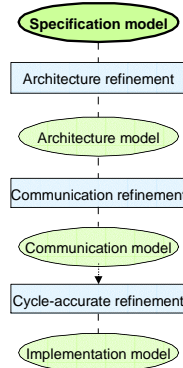
        ArchModel --> CommRef[Communication refinement]
        ProtoIP[(Proto. IP)] --> CommRef
        CommRef --> CommModel([Communication model])
        CommModel --> Comp3[Compilation]
        CommModel --> Val3[Validation Analysis Estimation]
        Comp3 --> Sim3([Simulation model])
        Val3 --> Sim3

        CommModel --> ImplModel([Implementation model])
        RTLIP[(RTL IP)] --> ImplModel
        RTOSIP[(RTOS IP)] --> ImplModel
        ImplModel --> Comp4[Compilation]
        ImplModel --> Val4[Validation Analysis Estimation]
        Comp4 --> Sim4([Simulation model])
        Val4 --> Sim4
    
```

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## Specification Model

- High-level, abstract model
  - Pure system functionality
  - Algorithmic behavior
  - No implementation details
- No implicit structure / architecture
  - Behavioral hierarchy
- Untimed
  - Executes in zero (logical) time
  - Causal ordering
  - Events only for synchronization



(Source: A. Gerstlauer)

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## Specification Language

- Specification model
  - PSM model of computation
  - Separation of communication and computation
  - Hierarchical network of behaviors and channels
- SpecC language
  - True superset of ANSI-C
    - ANSI-C plus extensions for HW-design
  - Support of all concepts needed in system design
    - Structural and behavioral hierarchy
    - Concurrency
    - State transitions
    - Communication
    - Synchronization
    - Exception handling
    - Timing
    - RTL

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## Specification Modeling Guidelines

- Specification model
  - First executable system model in the design flow
    - “Golden Model”
    - all other models will be derived from this one
  - High abstraction level
  - Separation of communication and computation
    - channels and behaviors
  - No implementation details
    - unrestricted exploration of design space
  - Pure functional
    - no structural information
  - No timing
    - exception: timing constraints

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## Specification Modeling Guidelines

- Computation: Behaviors
  - Hierarchy: explicit concurrency, state transitions, ...
  - Granularity: leaf behaviors = smallest indivisible units
  - Encapsulation: localization, explicit dependencies
  - Concurrency: explicitly specified (par, pipe, fsm, seq, ...)
  - Time: untimed, partial ordering
- Communication: Channels
  - Semantics: abstract communication, synchronization (standard channel library)
  - Dependencies: explicit data dependency, partial ordering, port connectivity

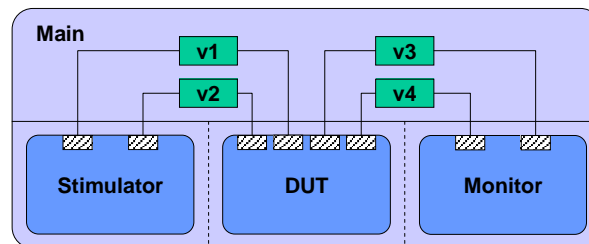
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## Specification Modeling Guidelines

- Modeling rules
  - Syntax and semantics
    - SpecC language, Version 2.0
  - Test bench (Stimulator, Monitor)
    - no restrictions in syntax and semantics (no synthesis)
  - DUT (Design under test)
    - restricted by syntax and semantic rules (for synthesis!)



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## Specification Modeling Guidelines

- Example rules for SpecC environment
  - Clean behavioral hierarchy
    - hierarchical behaviors:
      - no code other than par, pipe, seq, fsm, try-trap, ... statements
    - leaf behaviors:
      - no child behavior calls (basically pure ANSI-C code)
  - Clean communication
    - point-to-point communication via standard channels
    - ports of plain type or interface type, no pointers!
    - port maps to local variables or ports only
- Detailed rules for SpecC Environment
  - CECS Technical Report 03-21:
    - “*System-on-Chip Specification Style Guide*”
    - by A. Gerstlauer, K. Ramineni, R. Doemer, D. Gajski
  - [http://www.ics.uci.edu/~doemer/publications/CECS\\_TR\\_03\\_21.pdf](http://www.ics.uci.edu/~doemer/publications/CECS_TR_03_21.pdf)

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## Specification Modeling Guidelines

- C code conversion
  - Functions become behaviors or channels
  - Functional hierarchy becomes behavioral hierarchy
    - clean behavioral hierarchy required
    - if-then-else structure becomes FSM
    - while/for/do loops become FSM
  - Explicitly specify potential parallelism
  - Explicitly specify communication
    - avoid global variables
    - use local variables and ports (signals, wires)
    - use standard channels
  - Data types
    - avoid pointers, use arrays instead
    - use explicit SpecC data types if suitable

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## Specification Example

- Design example: GSM Vocoder
  - Enhanced full-rate voice codec
  - GSM standard for mobile telephony (GSM 06.10)
  - Lossy voice encoding/decoding
    - Incoming speech samples @ 104 kbit/s
    - Encoded bit stream @ 12.2 kbit/s
    - Frames of  $4 \times 40 = 160$  samples ( $4 \times 5\text{ms} = 20\text{ms}$  of speech)
  - Real-time constraint:
    - max. 20ms per speech frame  
(max. total of 3.26s for sample speech file)
  - SpecC specification model
    - 29 hierarchical behaviors (9 par, 10 seq, 10 fsm)
    - 73 leaf behaviors
    - 9139 formatted lines of SpecC code  
(~13000 lines of original C code, including comments)

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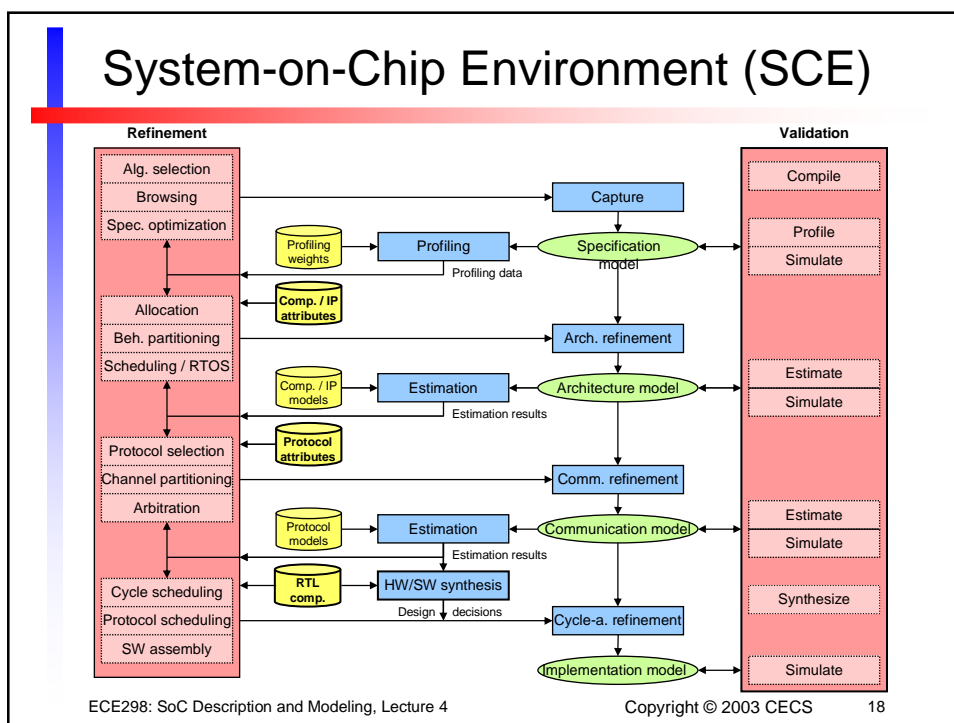
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## System-on-Chip Environment (SCE)

- SCE Components:
  - Graphical frontend (*sce*, *scchart*)
  - Editor (*sced*)
  - Compiler and simulator (*scc*)
  - Profiling and analysis (*scprof*)
  - Architecture refinement (*scar*)
  - RTOS refinement (*scos*)
  - Communication refinement (*sccr*)
  - RTL refinement (*scrtl*)
  - Software refinement (*sc2c*)
  - Scripting interface (*scsh*)
  - Tools and utilities ...

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## SCE Main Window

The screenshot displays the SCE Main Window interface. The top menu bar includes File, Edit, View, Project, Synthesis, Validation, Windows, and Help. The main workspace is divided into several panes:

- Design:** Shows a project tree for 'VocoderSpec.sir' with components like 'VocoderArch.sir', 'VocoderComm.sir', 'VocoderRTL.sir', and 'VocoderImpl.sir'.
- Open Loop - VocoderSpec - VocoderSpec.sir:** A detailed component hierarchy showing 'Main' containing 'Coder', 'Pre\_Process', 'Coder\_12K2', 'seq1', 'LP\_Analysis', 'Open Loop', 'Subframes', 'Update', 'Subframes\_End', 'Short\_Signals', 'Post\_Process', 'Monitor', and 'Stimulus'.
- Table:** A table listing components with their names, types, and computation times.
 

Name	Type	N	Computation [cycles]	Da [ct]
Open_Loop		163	257413	
syn_filter	Syn_Filter	3912	5226	
residual	Residu	1856	5777	
ol_lag_estimate	Ol_Lag_Est	163	222092	
for_init	Open_Loop_Init	163	0	
for_end	Open_Loop_End	652	81	
for_body2	Open_Loop_Body2	652	244	
for_body1	Open_Loop_Body1	652	1	
wp1	short int [80]			
p_speech_i	short int *			
mem_wv	short int [10]			
i	int			
A_U	short int [11]			
sp2	short int [11]			
sp1	short int [11]			
wp	inout short int *			
btbx_ctl	in unscaled bits[0]			
- Console:** Shows the output of the compilation process:
 

```

Compile: Simulate Analyze Refine Shell
Input: "VocoderSpec.o"
Output: "VocoderSpec.o"
Linking ...
Input: "VocoderSpec.o"
Output: "VocoderSpec"
Done.
      
```

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## SCE Source Editor

The screenshot shows the SCE Source Editor interface. On the left, a design tree displays the hierarchy of components, including 'VocoderSpec', 'VocoderArch', 'VocoderComm', 'VocoderRTL', and 'VocoderImpl'. The main window displays the behavioral code for 'Coder\_12k2\_Ses1'.

```

behavior Coder_12k2_Ses1(
  in  Word16 speech_proc[L_FRAME],
  Word16 old_speech[L_TOTAL],
  Word16 *speech,
  out  Word16 *p_window,
  Word16 old_wsp[L_FRAME + PIT_MK],
  out  Word16 *wsp,
  Word16 old_exc[L_FRAME + L_INTERPOL],
  out  Word16 *exc,
  out  Flag  patch,
  out  BitCtrl txdtx_ctrl,
  in  Flag  reset_flag
)

implements Ireset
{
void init(void)
{
  /* Initialize pointers to speech vector.
  */
  speech = old_speech + L_TOTAL - L_FRAME; /* New speech */
  p_window = old_speech + L_TOTAL - L_WINDOW; /* For LPC window */

  /* Initialize pointers */
  wsp = old_wsp + PIT_MK;
  exc = old_exc + PIT_MK + L_INTERPOL;
  /* vectors to zero */
  Set_zero (old_speech, L_TOTAL);
  Set_zero (old_exc, PIT_MK + L_INTERPOL);
  Set_zero (old_wsp, PIT_MK);
  txdtx_ctrl = TX_SP_FLAG | TX_VAD_FLAG;
  patch = 1;
}
}
    
```

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## SCE Hierarchy Displays

The first screenshot shows the 'Open\_Loop' hierarchy chart, which is a flow diagram with the following components: 'for\_init', 'for\_body1', 'for\_body2', 'weight\_w1', 'weight\_w2', 'residual', and 'sig\_jitter'. The second screenshot shows the 'Coder' hierarchy chart, which is a block diagram with inputs 'speech\_ctrls', 'exc\_flag', 'wsp', 'old\_exc', 'old\_wsp', and 'old\_speech', and outputs 'speech\_ctrls', 'exc\_flag', 'wsp', 'old\_exc', 'old\_wsp', and 'old\_speech'. It includes sub-blocks for 'DSP' and 'HW'.

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## SCE Compiler and Simulator

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## SCE Profiling and Analysis

Type	N	Computation [cycles]
code	Q_Gain_Code	852 8817
upd_sh	Ex_Syn_Upd_Sh	852 1250
		852 7387

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## Homework Assignment 2

- Administration
  - Server
    - `alpha.eecs.uci.edu`
    - Intel Pentium CPU, 2.4GHz, 1GB RAM
    - RedHat Linux 9
    - Access via Secure Shell (`ssh`)
  - Accounts
    - User ID same as your UCI ID
    - Password as discussed in class
  - Software
    - RedHat Source Navigator
      - `/opt/sourcenav-5.2b2/bin/snavigator`
    - CECS System-on-Chip Environment
      - `/opt/sce-20030530/bin/setup.csh`

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## Homework Assignment 2

- Tasks
  - Task 1:
    - Make yourself familiar with the SpecC compiler
      - Use `scc` to compile and run the examples found in `/opt/sce-20030530/examples/simple/`
  - Task 2:
    - Make yourself familiar with the SoC Environment
      - Go through the initial steps of the SCE tutorial found in `/opt/sce-20030530/doc/SCE_Tutorial/sce-tutorial.pdf`
  - Task 3:
    - Create an initial Specification Model with test bench for the MPEG-Audio example
      - Create an MPEG-Audio model with Stimulator, Decoder, and Monitor behaviors