

ECE 298: System-on-Chip Description and Modeling Lecture 9

Rainer Dömer

doemer@uci.edu

The Henry Samueli School of Engineering
Electrical Engineering and Computer Science
University of California, Irvine

Lecture 9: Overview

- UML and other SLDL
 - Invited Talk by Wolfgang Mueller, C-LAB
 - Discussion
- Homework Assignment 4
 - Status, Discussion
- Homework Assignment 5
 - Technical Report

Lecture 9: Overview

- UML and other SLDL
 - Invited Talk by Wolfgang Mueller, C-LAB
 - Discussion
- Homework Assignment 4
 - Status, Discussion
- Homework Assignment 5
 - Technical Report

UML and other SLDL

- Invited Talk by Dr. Wolfgang Mueller, C-LAB
 - Short Biography
 - 1996 Ph.D., University of Paderborn, Germany
 - Member of C-LAB, a joint R&D institute of
 - University of Paderborn, Germany
 - Siemens Business Services
 - Head of groups for
 - User Interfaces
 - Human-Computer Interaction
 - Visual Interactive Systems
 - Served in various program committees (e.g. DATE, FDL)
 - Authored more than 100 publications
 - Research interests
 - System design methodologies
 - System description languages
 - System integration technologies

Lecture 9: Overview

- UML and other SLDL
 - Invited Talk by Wolfgang Mueller, C-LAB
 - Discussion
- Homework Assignment 4
 - Status, Discussion
- Homework Assignment 5
 - Technical Report

Lecture 9: Overview

- UML and other SLDL
 - Invited Talk by Wolfgang Mueller, C-LAB
 - Discussion
- Homework Assignment 4
 - Status, Discussion
- Homework Assignment 5
 - Technical Report

Homework Assignment 4

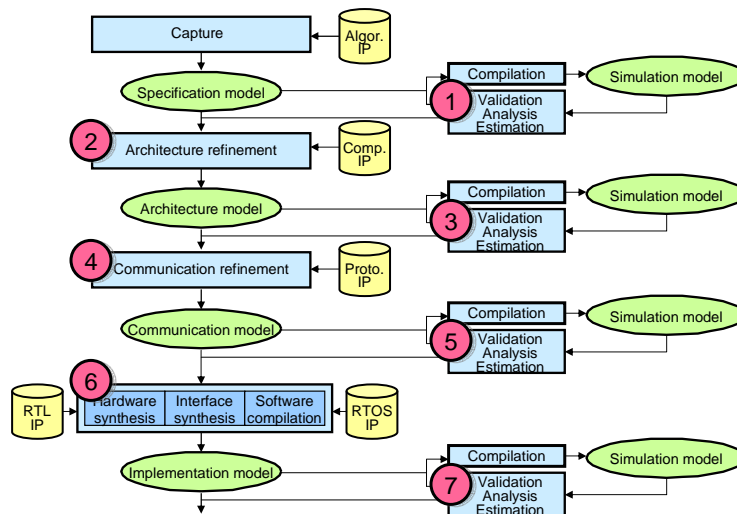
- Tasks
 - Task 1: Choose design example:
 - Option 1: MPEG-Audio Decoder (from previous homework)
 - Option 2: GSM Vocoder (from SCE tutorial)
 - Task 2: Design Space Exploration with SCE
 - Use different number and type of PEs
 - SW: Motorola DSP56600, Motorola Coldfire, Toshiba TX49
 - HW: Standard custom HW block
 - Memories: Motorola Coldfire Memory, Samsung KM684002
 - Use different clock frequencies (power savings!)
 - Use different mappings (behaviors to PEs, variables to memories)
 - Use different scheduling schemes (dynamic vs. static)
 - Estimate the performance and cost for each option
 - Task 3: Design Refinement with SCE
 - Generate the “best” system architecture for the design
 - Use straightforward communication, HW, SW design
- *Note/store all results for the final report!*

ECE298: SoC Description and Modeling, Lecture 9

(c) 2004 R. Doemer

7

Homework Assignment 4



ECE298: SoC Description and Modeling, Lecture 9

(c) 2004 R. Doemer

8

Lecture 9: Overview

- UML and other SLDL
 - Invited Talk by Wolfgang Mueller, C-LAB
 - Discussion
- Homework Assignment 4
 - Status, Discussion
- Homework Assignment 5
 - Technical Report

Homework Assignment 5

- Technical Report
 - Summarize the specification and implementation of a System-on-Chip design example
 - MPEG-Audio Decoder
 - GSM Vocoder (alternative)
 - Focus
 - Description and Modeling of Specification Model
 - Lessons learned in this class
 - Also
 - SoC Design Issues
 - Top-down Design flow
 - Design space exploration

Homework Assignment 5

- Technical Report, Skeleton of Contents
 1. Title page
 - *Title, authors, date*
 2. Introduction to SoC Design
 1. Challenges of SoC Design
 - *General SoC issues, problems and goals*
 2. SoC Specification
 - *Specification capture and modeling, goals*
 3. SoC Exploration
 - *Design flow, stages, exploration cycles*
 3. Design Example
 1. Description of the design example
 - *Background, area, algorithm, features*
 2. Source
 - *Origin, C code, properties*
 3. Design considerations
 - *Design constraints, requirements, goals*
 4. Specification capture
 1. Testbench
 - *Structure, conversion from C code, validation*
 2. Design Under Test
 - *Structure, hierarchy, parallelism, communication, properties, ...*
 5. ...

ECE298: SoC Description and Modeling, Lecture 9

(c) 2004 R. Doemer

11

Homework Assignment 5

- Technical Report, Skeleton of Contents
 5. Design space exploration
 1. System architecture
 - *Number and type of PEs, mapping*
 2. Scheduling
 - *Dynamic vs. static scheduling (if applicable)*
 3. Communication architecture
 - *Bus allocation, mapping (if applicable)*
 6. Implementation
 1. Software implementation
 - *Code generation (if applicable)*
 2. Hardware implementation
 - *Behavioral and RTL synthesis (if applicable)*
 3. Cycle-accurate model
 - *Final model, properties*
 7. Conclusion
 - *Concluding remarks, lessons learned*
 8. References
 - *Applicable literature*

ECE298: SoC Description and Modeling, Lecture 9

(c) 2004 R. Doemer

12