

EECS 221: System-on-Chip Software Synthesis Lecture 9

Rainer Dömer

doemer@uci.edu

The Henry Samueli School of Engineering
Electrical Engineering and Computer Science
University of California, Irvine

Lecture 9: Overview

- Course Administration
 - Final course evaluation
- Code Generation
 - Embedded Software Generation from SLDL
- Technical Report
 - SoC Software Synthesis of Monte-Carlo Example
- Outlook
 - Next course on SoC Design

Course Administration

- Final Course Evaluation
 - 8th through 10th week
 - Nov. 13, 2006, 8am through Dec. 3, 2006, 11:45pm
 - **Closes end of this week!**
 - Online via EEE Evaluation application
- Evaluation of Course and Instructor
 - Voluntary
 - Anonymous
 - Very valuable
- Help to improve this class!
 - **Please spend 5 minutes!**

EECS221: SoC Software Synthesis, Lecture 9

(c) 2006 R. Doemer

3

SoC Software Synthesis

- Code Generation
 - Embedded Software Generation from SLDL
 - automatically generate ANSI-C code from SpecC SLDL
 - Paper presented at ASPDAC 2004
 - Haobo Yu, Rainer Doemer, Daniel Gajski
 - *“Embedded Software Generation from System Level Design Languages”*

EECS221: SoC Software Synthesis, Lecture 9

(c) 2006 R. Doemer

4

SoC Software Synthesis

- Technical Report
 - Final deliverable for this course
 - Email electronic PDF file to doemer@uci.edu
 - Due: December 8, 2006, 2pm
 - Title
 - SoC Software Synthesis of Monte-Carlo Example
 - Contents
 - Describe the software synthesis approach
 - Use the Monte Carlo example as case study
 - Outline the major steps in the synthesis flow
 - Conclude with a summary of the lessons learned
 - Length
 - no more than 10 pages (plus appendix)

SoC Software Synthesis

- Technical Report: Suggested Outline
 - Title page
 - Project title, author, abstract
 - Introduction
 - Growing importance of embedded SW in SoC design
 - Top-down embedded SW design flow using SCE
 - SW Synthesis of a Monte Carlo Example
 - Specification model
 - Example validation through simulation
 - Architecture mapping, architecture model
 - Scheduling refinement, scheduled model
 - Network and link refinement, communication model
 - C code generation, C model
 - Cross compilation, ISS model
 - Conclusion
 - Results, summary
 - Lessons learned
 - References
 - Appendix
 - SpecC source code of the example

Outlook

- Next course on System-on-Chip Design
 - Spring Quarter '07: EECS 221
 - “*System-on-Chip Design and Exploration*”
 - Instructor: Daniel D. Gajski