EECS 298: System-on-Chip Description and Modeling Lecture 5

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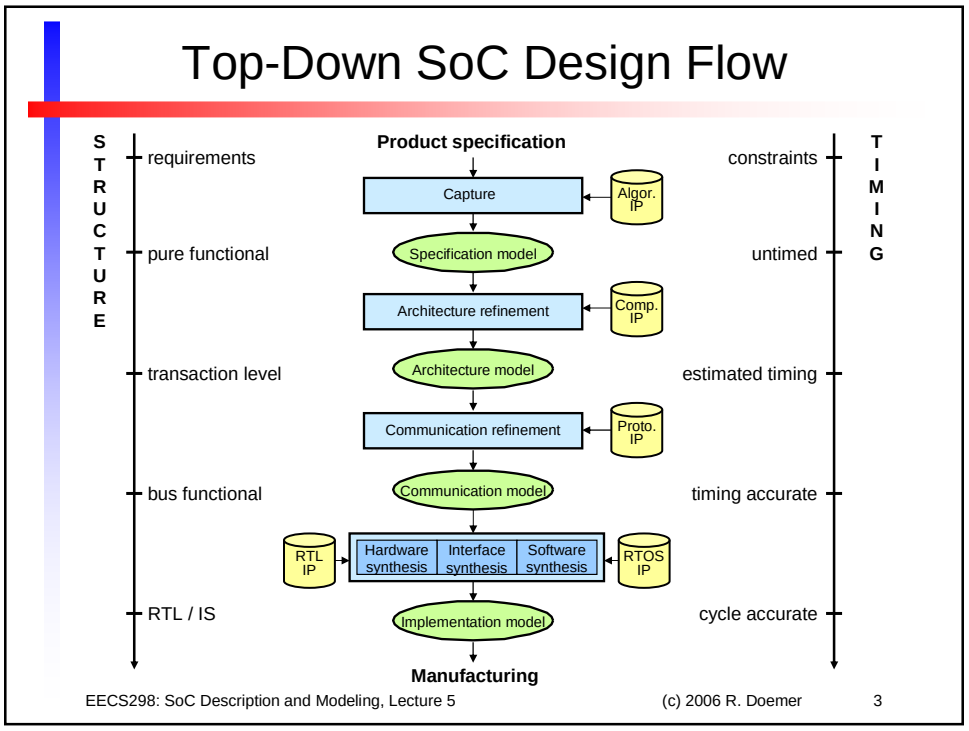
Lecture 5: Overview

- Top-Down SoC Design Methodology
  - Specification model
  - Architecture model
  - Communication model
  - Implementation model
- Homework Assignment 2
  - Discussion


Top-Down SoC Design Flow
STRUCTURE
TIMING
requirements
pure functional
transaction level
bus functional
RTL / IS
constraints
untimed
estimated timing
timing accurate
cycle accurate
Product specification
Capture
Algor. IP
Specification model
Architecture refinement
Comp. IP
Architecture model
Communication refinement
Proto. IP
Communication model
RTL IP
Hardware synthesis
Interface synthesis
Software synthesis
RTOS IP
Implementation model
Manufacturing
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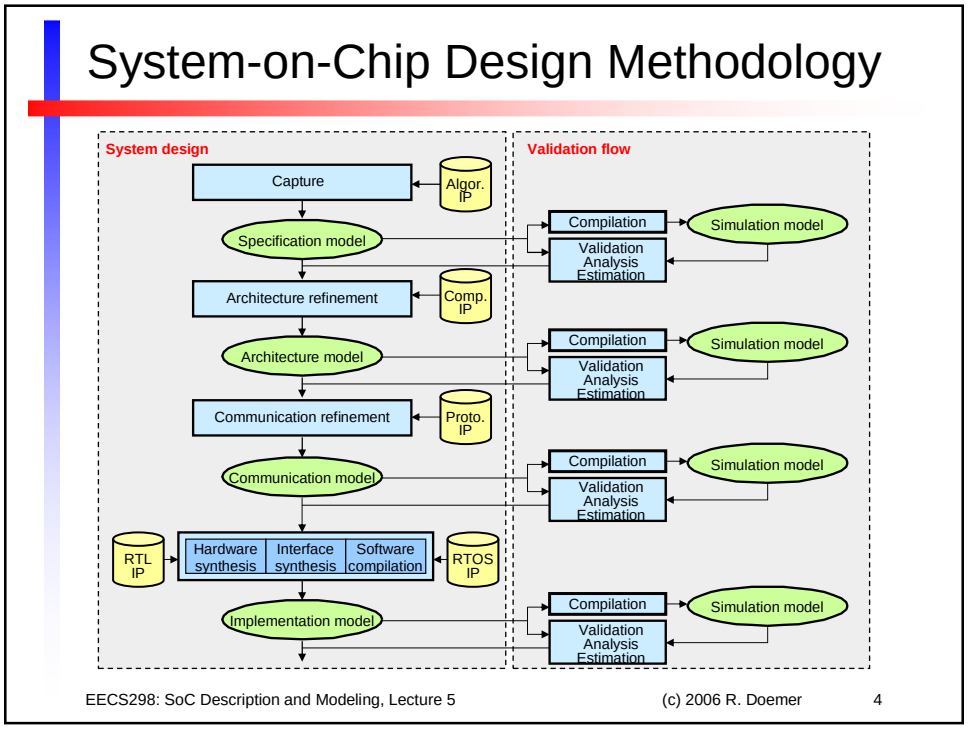
System-on-Chip Design Methodology
System design
Validation flow
Capture
Algor. IP
Specification model
Architecture refinement
Comp. IP
Architecture model
Communication refinement
Proto. IP
Communication model
RTL IP
Hardware synthesis
Interface synthesis
Software compilation
RTOS IP
Implementation model
Compilation
Validation Analysis Estimation
Simulation model
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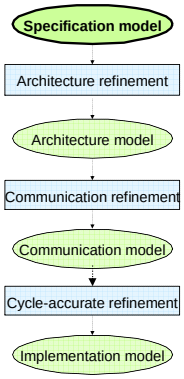
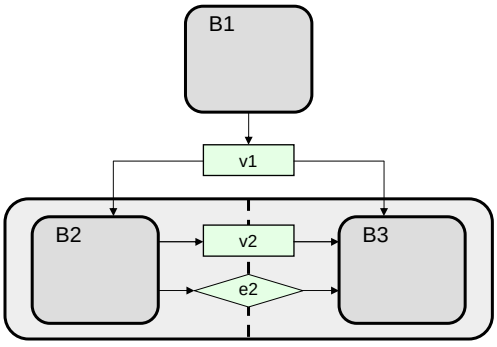
Specification Model

- High-level, abstract model
  - Pure system functionality
  - Algorithmic behavior
  - No implementation details
- No implicit structure / architecture
  - Behavioral hierarchy
- Untimed
  - Executes in zero (logical) time
  - Causal ordering
  - Events only for synchronization



(Source: A. Gerstlauer)

Specification Model Example

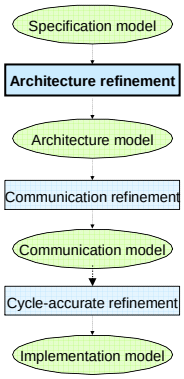


- Simple, typical specification model
  - Hierarchical parallel-serial composition
  - Communication through ports and variables, events

(Source: A. Gerstlauer)

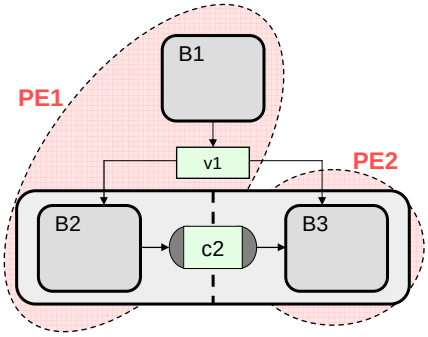
Architecture Refinement

- Component allocation / selection
- Behavior partitioning
- Variable partitioning
- Scheduling



(Source: A. Gerstlauer)

Allocation, Behavior Partitioning

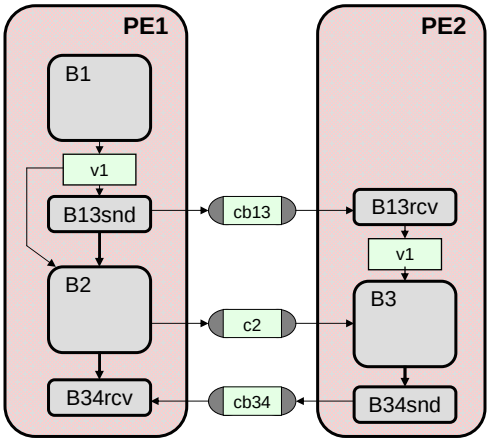


- Allocate PEs
- Partition behaviors
- Globalize communication

➢ Additional level of hierarchy to model PE structure

(Source: A. Gerstlauer)

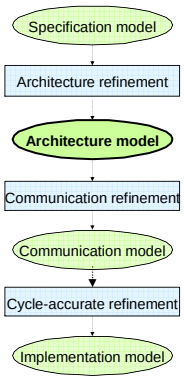
Architecture Model Example



(Source: A. Gerstlauer)

Architecture Model

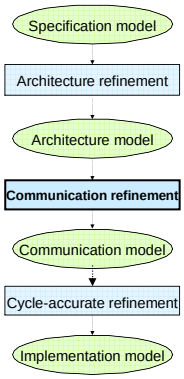
- Component structure/architecture
  - Top level of behavior hierarchy
- Behavioral/functional component view
  - Behaviors grouped under top-level component behaviors
  - Sequential behavior execution
- Timed
  - Estimated execution delays



(Source: A. Gerstlauer)

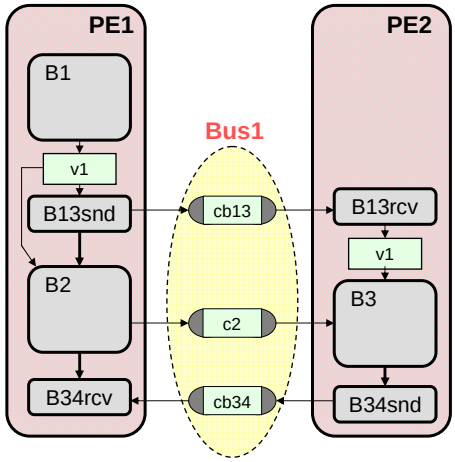
Communication Refinement

- Bus allocation / protocol selection
- Channel partitioning
- Protocol, transducer insertion
- Inlining



(Source: A. Gerstlauer)

Bus Allocation / Channel Partitioning

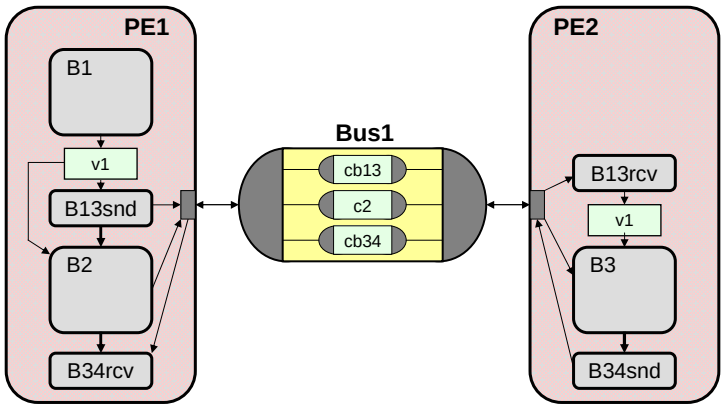


- Allocate busses
- Partition channels
- Update communication

➢ Additional level of hierarchy to model bus structure

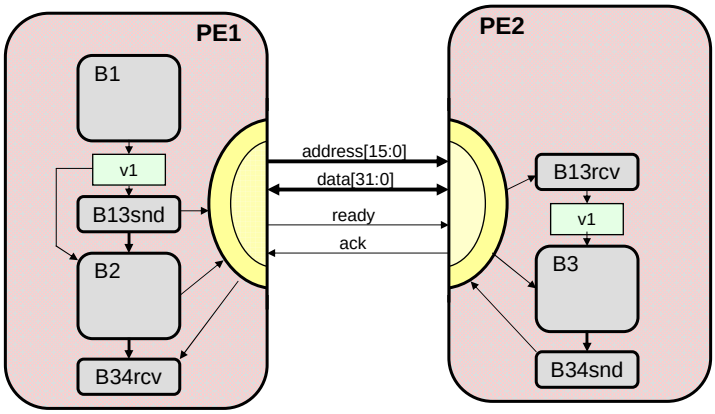
(Source: A. Gerstlauer)

Model after Channel Partitioning



(Source: A. Gerstlauer)

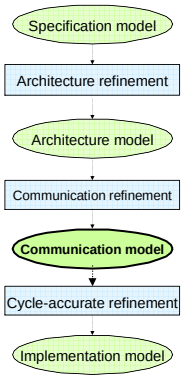
Communication Model Example



(Source: A. Gerstlauer)

Communication Model

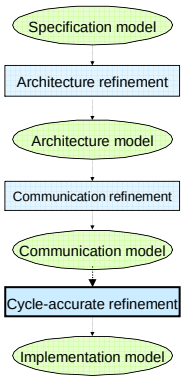
- Component & bus structure/architecture
  - Top level of hierarchy
- Bus-functional component models
  - Timing-accurate bus protocols
  - Behavioral component description
- Timed
  - Estimated component delays



(Source: A. Gerstlauer)

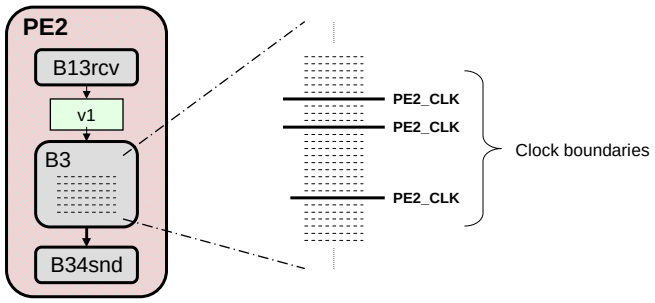
Cycle-accurate Refinement

- Clock-accurate implementation of PEs
  - Hardware synthesis
  - Software synthesis
  - Interface synthesis



(Source: A. Gerstlauer)

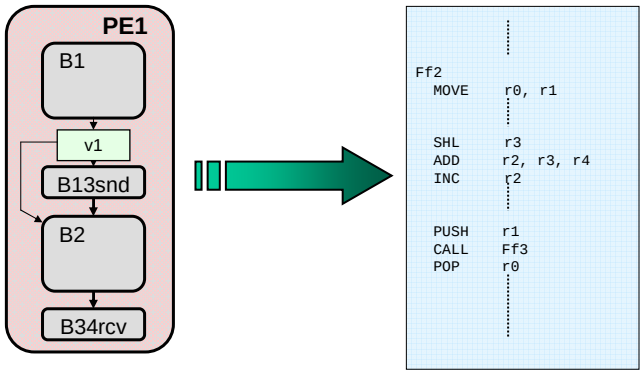
Hardware Synthesis



- Schedule operations into clock cycles
  - Define clock boundaries in leaf behavior C code
  - Create FSMD model from scheduled C code

(Source: A. Gerstlauer)

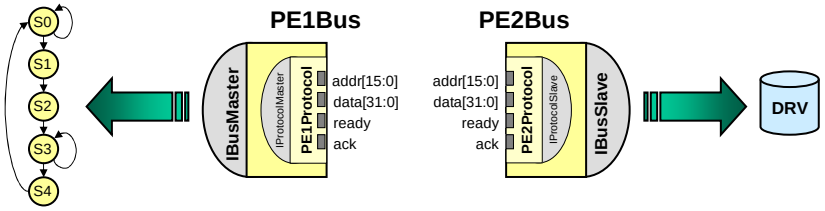
Software Synthesis



- Implement behavior on processor instruction-set
  - Code generation
  - Compilation

(Source: A. Gerstlauer)

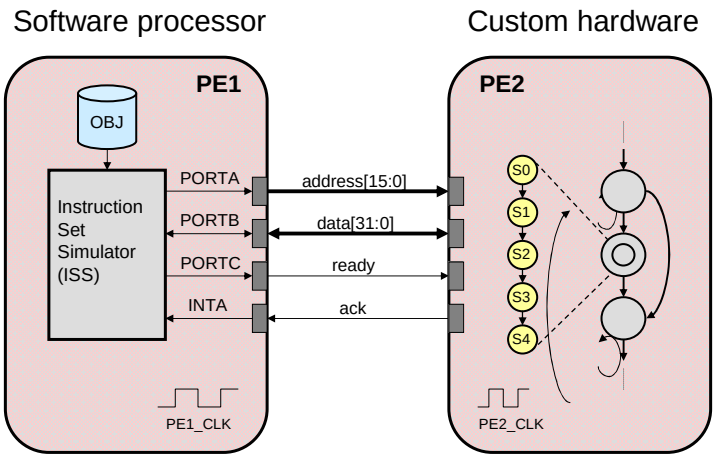
Interface Synthesis



- Implement communication on components
  - Hardware bus interface logic
  - Software bus drivers

(Source: A. Gerstlauer)

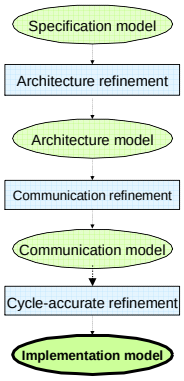
Implementation Model Example



(Source: A. Gerstlauer)

Implementation Model

- Cycle-accurate system description
  - RTL description of hardware
    - Behavioral/structural FSMD view
  - Object code for processors
    - Instruction-set co-simulation
  - Clocked bus communication
    - Bus interface timing based on PE clock



(Source: A. Gerstlauer)

System-on-Chip Design Methodology

- Four levels of abstraction
  - Specification model: untimed, functional
  - Architecture model: estimated, structural
  - Communication model: timed, bus-functional
  - Implementation model: cycle-accurate, RTL/IS
- Three refinement steps
  - Architecture refinement
  - Communication refinement
  - Cycle-accurate refinement
    - HW / SW / interface synthesis
- Well-defined, formal models & transformations
  - Automatic, gradual refinement
  - Executable models, test bench re-use
  - Simple verification

(Source: A. Gerstlauer)

Homework Assignment 2: Discussion

- Project
  - Elevator Control System (ECS)
    - Distributed embedded system
    - Set of communicating Elevator Control Units (ECU)
- Tasks for System Specification
  - Decompose ECS into multiple ECUs
  - Develop a specification model for each ECU
  - Validate each ECU model using simulation
  - Compose entire ECS using developed ECUs
  - Validate entire ECS
  - Then, refine and implement ECS...

Homework Assignment 2: Discussion

- Decomposition of ECS
  - Floor panel
    - panel at each floor and each shaft with up/down controls
  - Floor display
    - display of current floor and direction at each floor
  - Floor door
    - Control unit to open/close doors at each floor
  - Car panel
    - panel in each car with request controls
  - Car display
    - display of current floor and direction in each car
  - Car door
    - Control unit to open/close doors in each car
  - Main control unit
    - central control unit to control the entire ECS
  - Motor control unit
    - control unit for the motor atop each shaft

Homework Assignment 2: Discussion

- Deliverables
  - Specification document for one ECU
    - Illustration figure
    - Schematic view of ECU SoC with ports
    - Brief (!) description of functionality (in English)
  - Executable specification model for one ECU embedded in proper test bench (using SpecC)
  - Successful simulation run
- Due
  - Week 5 (next week)