EECS 298: System-on-Chip Description and Modeling Lecture 6

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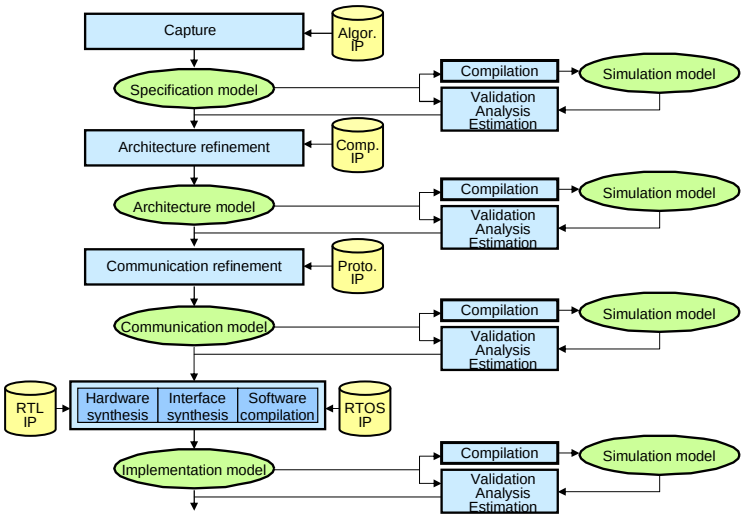
Lecture 6: Overview

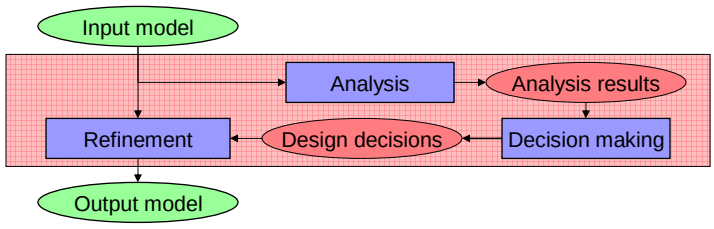
- SoC Design Methodology
- SoC Model Refinement
- Automating the SoC Design Flow
- SoC Architecture Exploration
  - Refinement Decisions
- SoC Communication Exploration
  - Refinement Decisions
- Automatic Model Refinement
  - Example
- Homework Assignment: Discussion

SoC Design Methodology



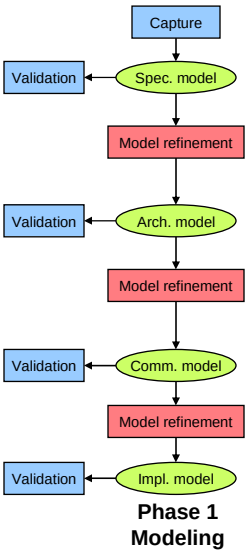
SoC Model Refinement

- Every step in the design process includes
  - Model refinement
  - Model analysis
  - Decision making

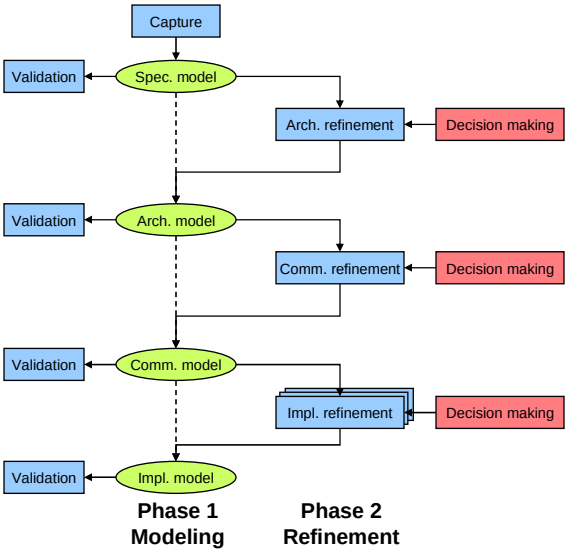


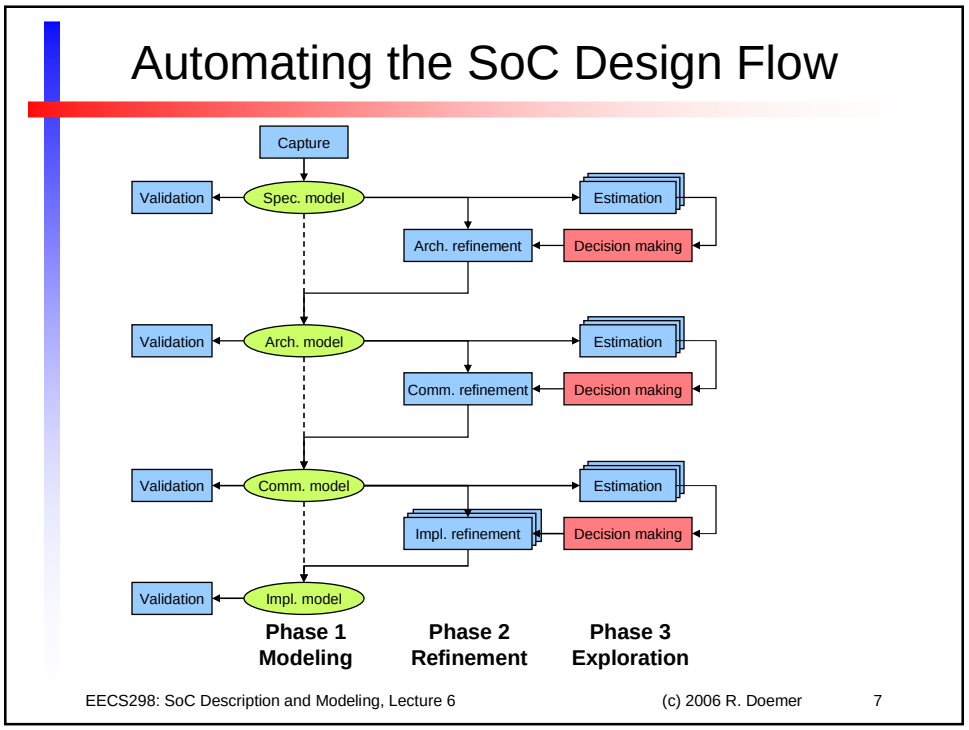
  - Synthesis = Analysis + Decision Making + Refinement

Automating the SoC Design Flow



Automating the SoC Design Flow




Automating the SoC Design Flow
Capture
Validation
Spec. model
Estimation
Arch. refinement
Decision making
Validation
Arch. model
Estimation
Comm. refinement
Decision making
Validation
Comm. model
Estimation
Impl. refinement
Decision making
Validation
Impl. model
Phase 1 Modeling
Phase 2 Refinement
Phase 3 Exploration
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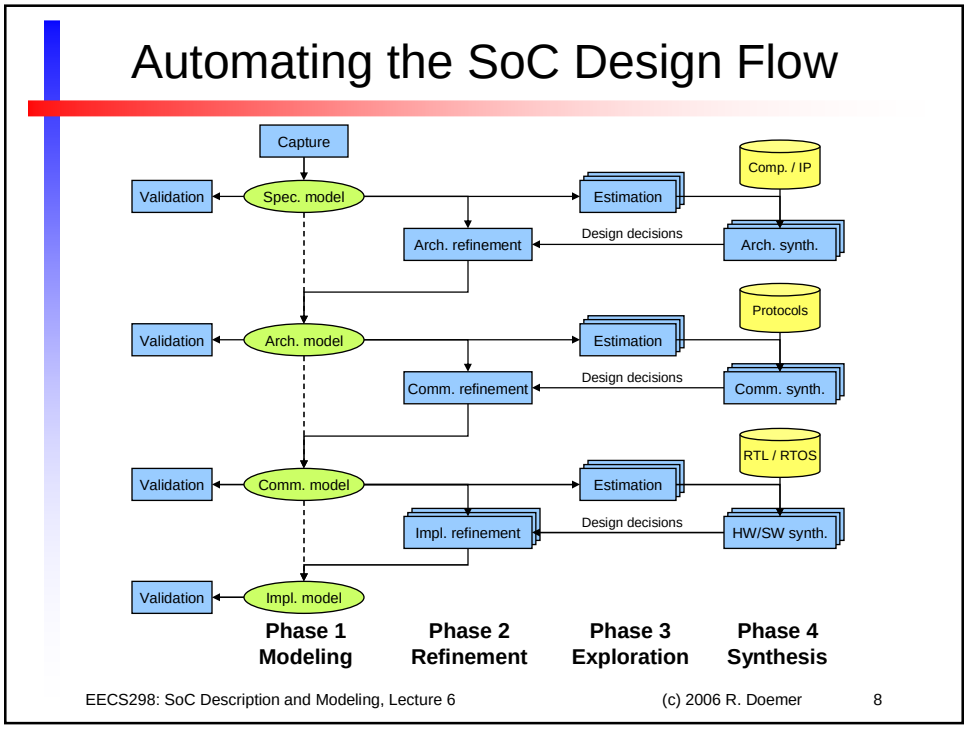
Automating the SoC Design Flow
Capture
Comp. / IP
Validation
Spec. model
Estimation
Design decisions
Arch. refinement
Arch. synth.
Protocols
Validation
Arch. model
Estimation
Design decisions
Comm. refinement
Comm. synth.
RTL / RTOS
Validation
Comm. model
Estimation
Design decisions
Impl. refinement
HW/SW synth.
Validation
Impl. model
Phase 1 Modeling
Phase 2 Refinement
Phase 3 Exploration
Phase 4 Synthesis
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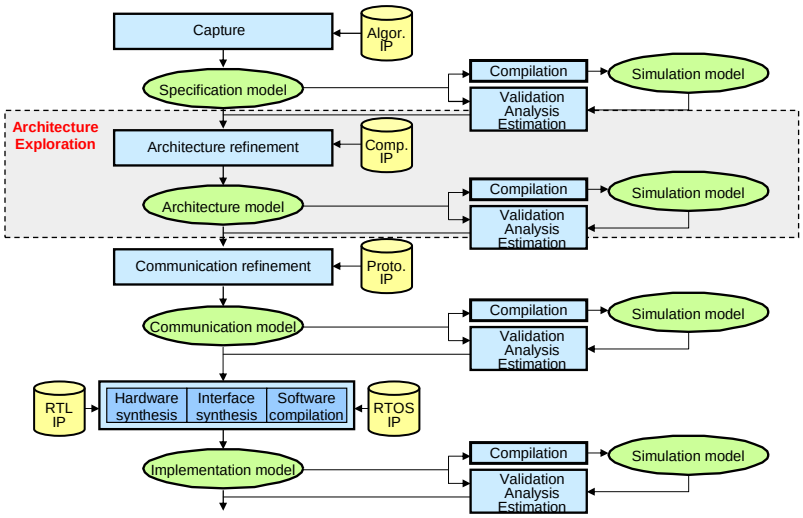
SoC Design Methodology



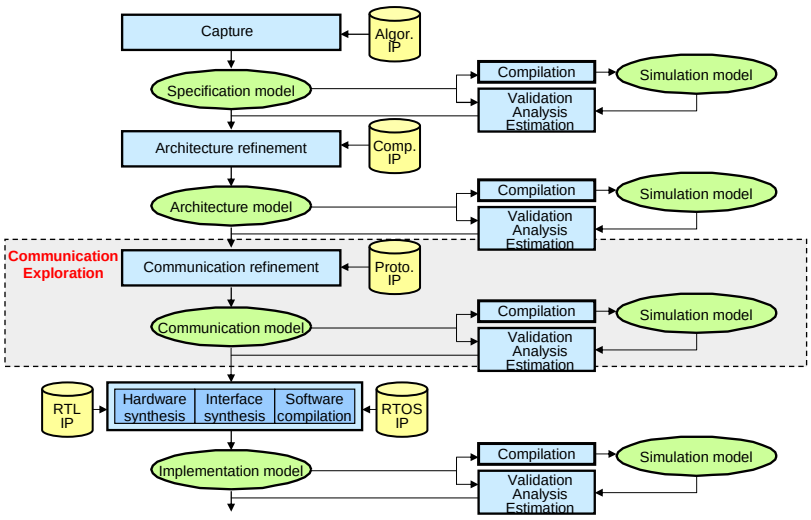
SoC Architecture Exploration

- Step 1: Architecture Decisions
  - Allocation of Processing Elements (PE)
    - Type and number of processors
    - Type and number of custom hardware blocks
    - Type and number of system memories
  - Mapping to PEs
    - Map each behavior to a PE
    - Map each channel to a PE
    - Map each variable to a PE
  - Result:
    System architecture of concurrent PEs
    with abstract communication in channels

SoC Architecture Exploration

- Step 2: Scheduling Decisions
  - For each PE, serialize the execution of behaviors to a single thread of control
  - Option (a): Static scheduling
    - For each set of concurrent behaviors, determine fixed order of execution
  - Option (b): Dynamic scheduling by RTOS
    - Choose scheduling policy, i.e. Round-robin or priority-based
    - For each set of concurrent behaviors, determine scheduling priority
  - Result: System model with abstract RTOS scheduler inserted in each PE

SoC Design Methodology



SoC Communication Exploration

- Communication Decisions
  - Allocation of system busses
    - Type and number of system busses
    - Type of bus protocol for each bus (if applicable)
    - Number of transducers (if applicable)
    - System connectivity
  - Mapping of channels to busses
    - Map each communication channel to a system bus (or multiple busses, if applicable)
  - Result:
    Bus-functional model of the system

Automatic Model Refinement

- Example:
  - System-on-Chip Environment (SCE)
  - GSM Vocoder design
- Online demonstration ...

Homework Assignment 2: Discussion

- Project
  - Elevator Control System (ECS)
    - Distributed embedded system
    - Set of communicating Elevator Control Units (ECU)
- Tasks for System Specification
  - Decompose ECS into multiple ECUs
  - Develop a specification model for each ECU
  - Validate each ECU model using simulation
  - Compose entire ECS using developed ECUs
  - Validate entire ECS
  - Then, refine and implement ECS...

Homework Assignment 2: Discussion

- Decomposition of ECS
  - Floor panel
    - panel at each floor and each shaft with up/down controls
  - Floor display
    - display of current floor and direction at each floor
  - Floor door
    - Control unit to open/close doors at each floor
  - Car panel
    - panel in each car with request controls
  - Car display
    - display of current floor and direction in each car
  - Car door
    - Control unit to open/close doors in each car
  - Main control unit
    - central control unit to control the entire ECS
  - Motor control unit
    - control unit for the motor atop each shaft

Homework Assignment 2: Discussion

- Deliverables
  - Specification document for one ECU
    - Illustration figure
    - Schematic view of ECU SoC with ports
    - Brief (!) description of functionality (in English)
  - Executable specification model for one ECU embedded in proper test bench (using SpecC)
  - Successful simulation run
- Due
  - Week 5 (next week)