Assignment 6

- Design Space Exploration
  1. Timing back-annotation
     - Manual insertion of estimated computation delays
       - Start from “perfect” specification model
         - » **`jpegencoder.sc`**
       - Add timing statements (**`waitfor`** after **`port.receive()`**)
         - » ChenDCT1: 10411200ns / 180
         - » ChenDCT2: 10411200ns / 180
         - » Quantize: 7839030ns / 180
         - » Zigzag: 2316600ns / 180
         - » Huffman: 8882810ns / 180
       - Save as timed model
         - » **`JpegTimed.sc`**
     - When executed, the resulting model should end at time 10574ms:
       - **`10574: Monitor exits simulation.`**

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- Design Space Exploration
  2. Architecture Exploration
     - Explore various system architectures
       - Use only ARM_7TDMI processors
       - Use only 100MHz core clock frequency
       - Use only 50MHz AMBA AHB bus
       - Vary between 1 and 5 CPUs
       - Vary the mapping of blocks in the DUT to CPUs
     - Note:
       Do not let the architecture refinement tool insert additional timing!
     - Example:
       - Use 3 CPUs, ARM1, ARM2, and ARM3
       - Map DCT1 to ARM1
       - Map DCT2 to ARM2
       - Map Quantize, Zigzag, and Huffman to ARM3
     - Note:
       Without scheduling, any architecture model will end at time 10574ms

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- Design Space Exploration
  3. Scheduling Exploration
     - Explore various scheduling strategies for each selected CPU
     - Choose from
       - Static scheduling
         - » with varying execution order
       - Round-Robin scheduling
       - Priority-based scheduling
         - » with varying priorities
     - Example:
       - 3 ARM CPUs with mapping as above
       - ARM1 statically scheduled
       - ARM2 statically scheduled
       - ARM3 scheduled with Round-Robin
     - When executed, the example model should end at time 19154ms

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4. Deliverable
   - Text file "**`JPEG_Exploration.txt`**" with table:
     - "Best" mapping and scheduling for architecture with 1 CPU
     - "Best" mapping and scheduling for architecture with 2 CPUs
     - "Best" mapping and scheduling for architecture with 3 CPUs
     - "Best" mapping and scheduling for architecture with 4 CPUs
     - "Best" mapping and scheduling for architecture with 5 CPUs
   - For each "best" architecture above, note the overall execution time in the table.

- Due
  - by Friday, Nov 14, 2008, at noon
  - by email to **`doemer@uci.edu`** with subject "EECS222C HW6"