System Level Design of JPEG Encoder

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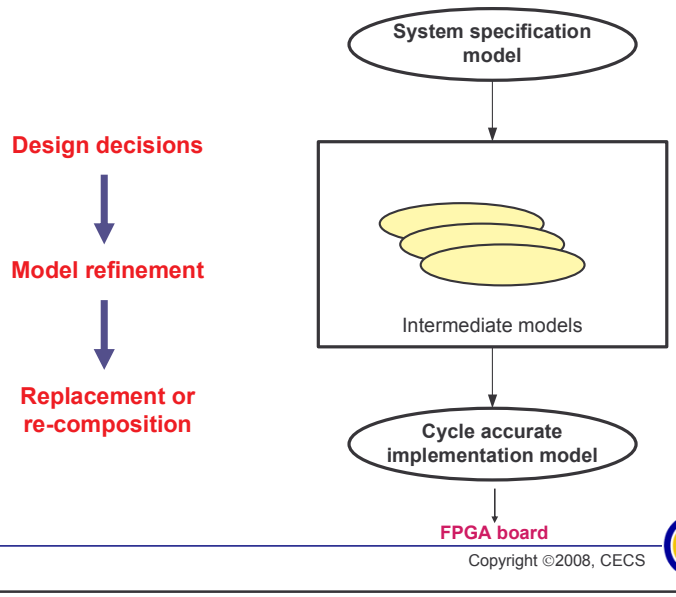
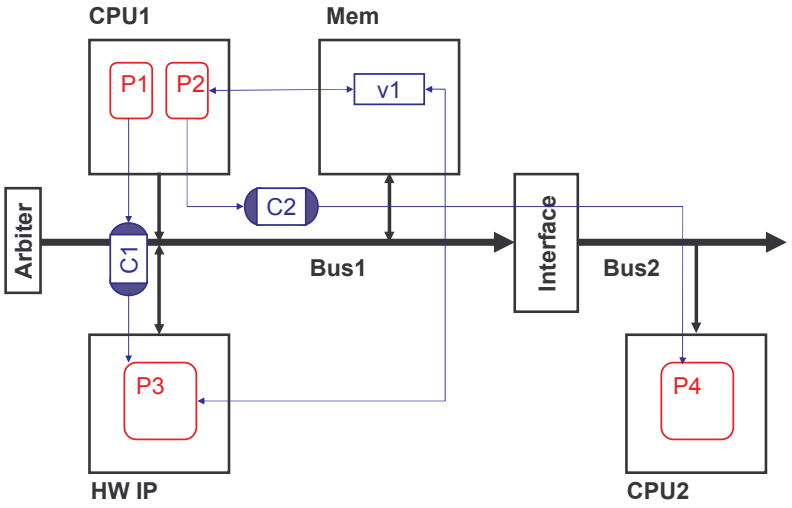
System Level Design Methodology

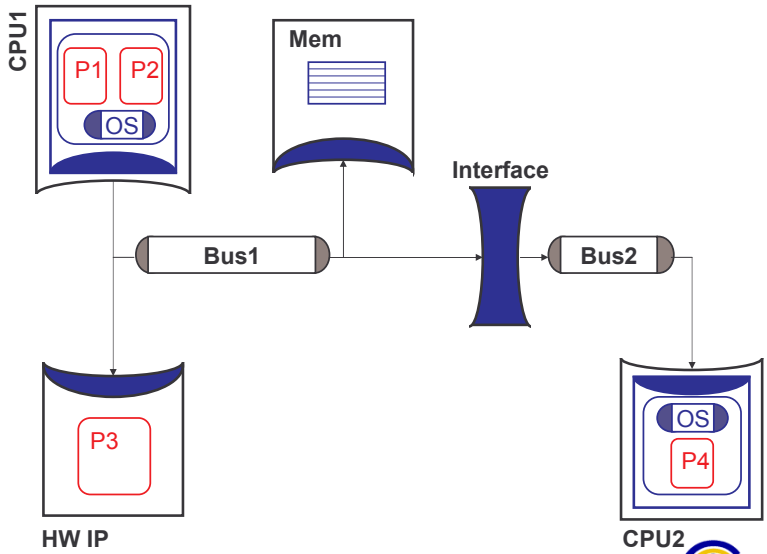


Input: System Definition

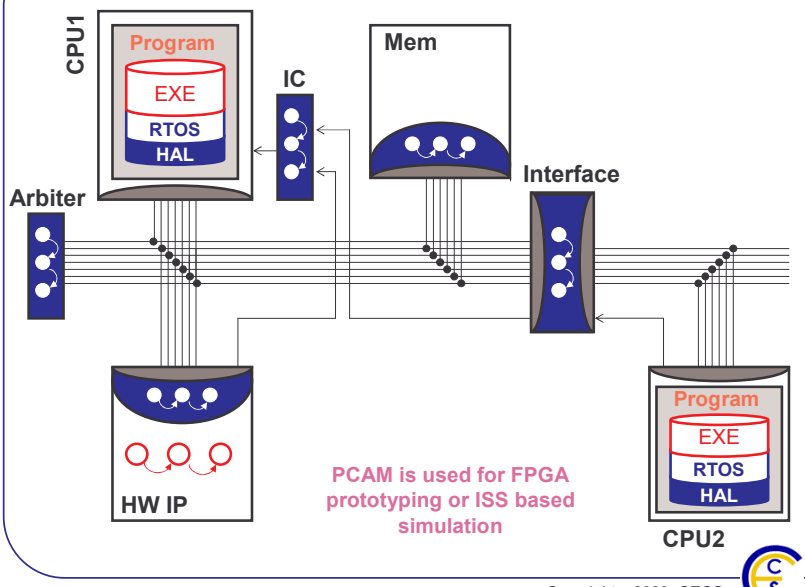


System Definition = *Platform* + *Application*

Intermediate System Level Model



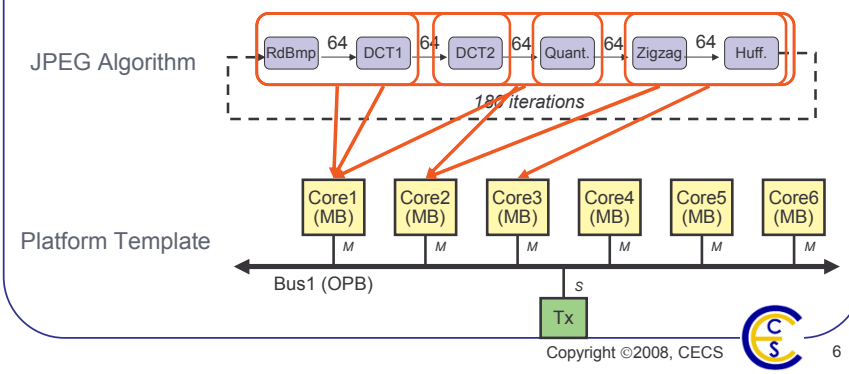
Pin/Cycle-Accurate Model



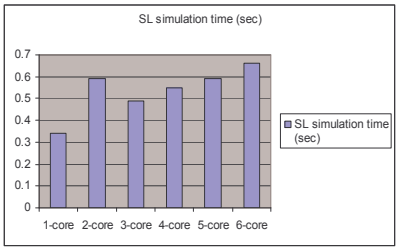
PCAM is used for FPGA prototyping or ISS based simulation

Design Example: JPEG Encoder

- **Multi-core platform implementation on Xilinx Virtex-4**
  - 1-6 Microblaze soft-cores with BRAM memory
  - Shared OPB bus with Transaction Buffer (Tx)
- **Application suitable for pipelining**
  - Transformed from sequential to pipelined for mapping

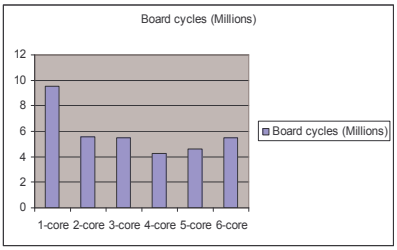


Results: System Level Simulation



- Native system level simulation is FAST
  - <1 sec for all designs at system level
  - >3 min. for Xilinx Virtual Platform (XVP) simulation for 1 core
  - >16 hrs for RTL simulation
- System level models support EARLY optimization
  - System level models are smaller, abstract and easy to debug
  - System level model compilation in <10 sec.
  - ~ days for RTL coding, >2 hours of FPGA synthesis

Results: Multi-core performance



- Increasing #cores gives performance improvement
  - Application is pipelined
  - Stages are executed concurrently on independent PEs
  - But communication overhead can be a factor
- Communication design
  - More stages → More concurrent communication
  - Shared bus has huge overhead for arbitration
  - Use multiple buses, P2P serial links