

## Project Discussion: Assignment 6

- Design Space Exploration using SCE
  1. Profile, analyze, estimate the digicam model (`jpegencoder3.tar.gz`)
    - For a single ARM\_7TDMI CPU at 100MHz
    - For metric of "Computation"
    - For blocks `read`, `dct`, `quant`, `huff`, `write`
    - Create a bar chart of the Computation Profile
      - "`ARM100.pdf`"
  2. Create a software-only reference model
    - Allocate and Map
      - 1 ARM7TDMI CPU at 100MHz as "ARM100" for JpegEncoder
      - 1 Custom HW\_Standard block at 100Mhz as "InputUnit" for ReadBlock
      - 1 Custom HW\_Standard block at 100Mhz as "OutputUnit" for WriteBlock
    - Estimate the allocation (Validation->Evaluate)
    - Perform Architecture Refinement
    - Perform Scheduling Refinement
      - Use Round-Robin scheduling policy on ARM100
    - When executed, the resulting model should encode our test picture in 39.252ms

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- Design Space Exploration
  3. Architecture Exploration
    - Explore various other system architectures
      - Use up to 5 ARM\_7TDMI processors
        - » Clock frequency may be 100, 150, or 200MHz
        - » Cost is assumed at \$100, \$150, \$200, respectively
        - » Use only 50MHz AMBA AHB bus
      - Use up to 5 HW\_Standard accelerator blocks
        - » Clock frequency may be 100, 200, 300, or 400MHz
        - » Cost is assumed at \$200, \$400, \$600, \$800, respectively
      - Vary the mapping of blocks in the DUT to CPUs and HW units
      - Vary the scheduling policy as needed
    - Example:
      - Use 1 HW100 for DCT
      - Use 1 ARM100 for everything else

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## Project Discussion: Assignment 6

- Design Space Exploration
  4. Scheduling Exploration
    - Explore various scheduling strategies for each selected CPU
    - Choose from
      - Static scheduling
        - » with varying execution order
      - Round-Robin scheduling
      - Priority-based scheduling
        - » with varying priorities
    - Example:
      - ARM100 scheduled with round-robin
      - ARM200 scheduled with priority-based scheduling
      - Static scheduling on HW blocks

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- Design Space Exploration
  5. Deliverables
    - Bar chart of the software-only computation profile
      - "ARM100.pdf"
    - Text file with table of 3 "good" architectures
      - List the allocation and mapping for each block
      - Simulate to estimate the resulting encoding delay
      - Calculate the assumed cost of the architecture
  - Due
    - by Friday, Nov 20, 2009, 2pm
    - by email to [doemer@uci.edu](mailto:doemer@uci.edu) with subject "EECS222A HW6"
    - bring a copy for discussion in class!

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