Assignment 6

1. Refinement of the MP3 Decoder model in SCE
   - Continue from “Spec” model of previous assignment
   - Select an appropriate system architecture
     - 1 ARM_7TDMI or LEON3 CPU at 50 MHz
     - 0-6 HW_Standard accellerators at 100 MHz
   - Perform the following refinement steps
     - Architecture Refinement
     - Scheduling Refinement
     - Network Refinement
     - Communication Link Refinement
       - Transaction-level model (TLM)
       - Pin-accurate model (PAM)
     - Reference instructions:
       - **`/home/doemer/EECS222C/Assignment6.txt`**
   - Deliverable:
     - Text file “**`refinement.txt`**” with
       - short description of the chosen target architecture
       - simulated execution times of each model
   - Due:
     - by Friday, Nov 12, 2010, at noon
     - by email to **doemer@uci.edu**, with subject “EECS222C HW6”