Embedded System Design: Modeling

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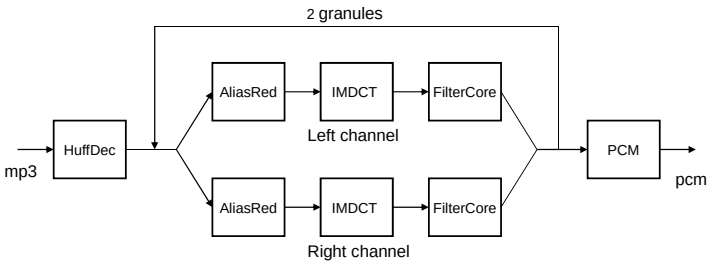
Outline

- Requirements
- **Modeling**
  - Introduction
  - Languages and models
  - System modeling semantics
  - Automatic model generation
  - **Design example**
  - Tools
  - Summary and conclusions
- Verification and synthesis
- Summary, conclusions and outlook

Example: MP3 Decoder

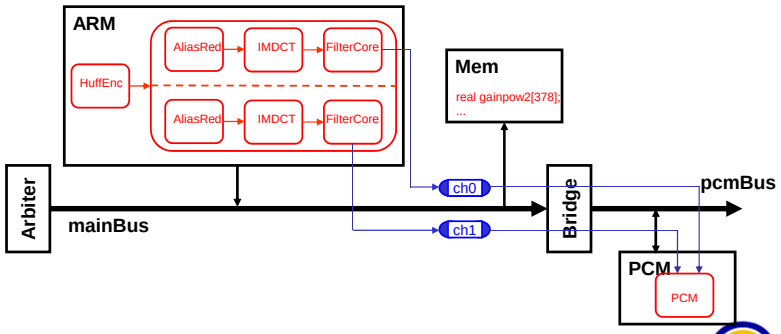
- **Functional block diagram (major blocks only)**



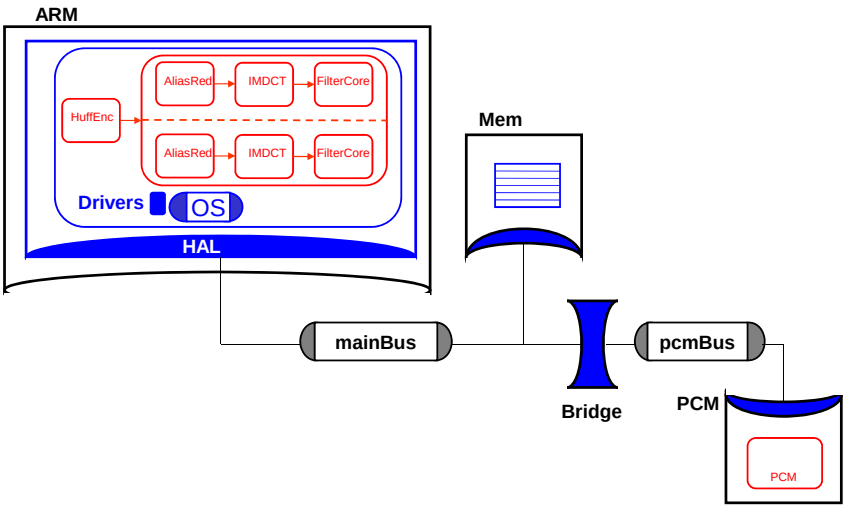
- **Timing constraints**
  - 38 frames per second
  - Frame delay < 26.12ms

System Definition

- **Components allocated from database**
- **Hierarchical processes inside PEs**
  - Parallel, sequential, leaf (C code)
- **Channels and variables between PEs**
- **Bridge used to interface two busses**



Output: Transaction-Level Model (TLM)



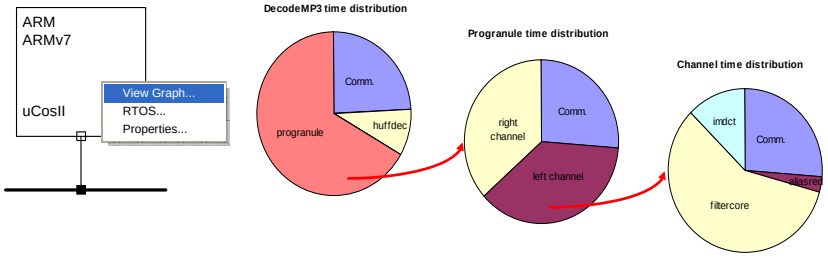
TLM Simulation

- **Timed-simulation**
  - Computation delays back-annotated in processes
  - Communication delays modeled in the bus channels
- **Simulation of TLM**
  - Functionally correct but frame delay far exceeds timing constraint

```
Terminal
File  Edit  View  Terminal  Tabs  Help
***
*** Simulating MP3DecoderDEMO1_Tlm ...
***
./MP3DecoderDEMO1_Tlm ./testStream//spot1.mp3 MP3DecoderDEMO1_Tlm.pcm ./testStre
am//spot1.txt
 Input MP3file:  ./testStream//spot1.mp3
 Output bitstream file:  MP3DecoderDEMO1_Tlm.pcm
Bitrate = 96000 bits/sec, Sampling frequency = 44100 Samples/Sec
Initial Latency = 4.73 ms
Missed deadline per frame at frame 2 35.98 > 26.12
Missed deadline per frame at frame 3 35.98 > 26.12
***
*** Checking MP3DecoderDEMO1_Tlm.pcm for correctness...
***
diff -s ./testStream//spot1.pcm MP3DecoderDEMO1_Tlm.pcm
Files ./testStream//spot1.pcm and MP3DecoderDEMO1_Tlm.pcm are identical
***
*** Simulation successful!
***
```

Computation Analysis

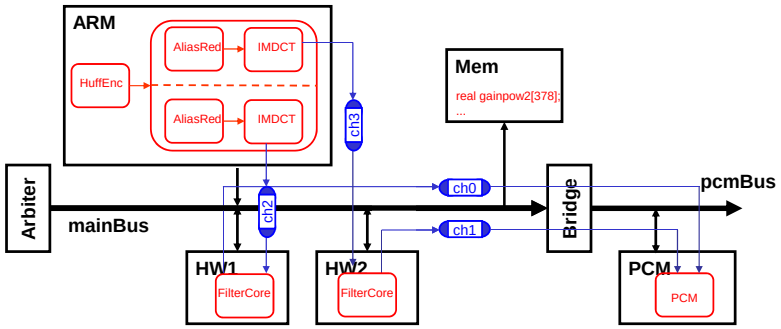
- **View computation time of processes**
  - *FilterCore* is the most computation-intensive



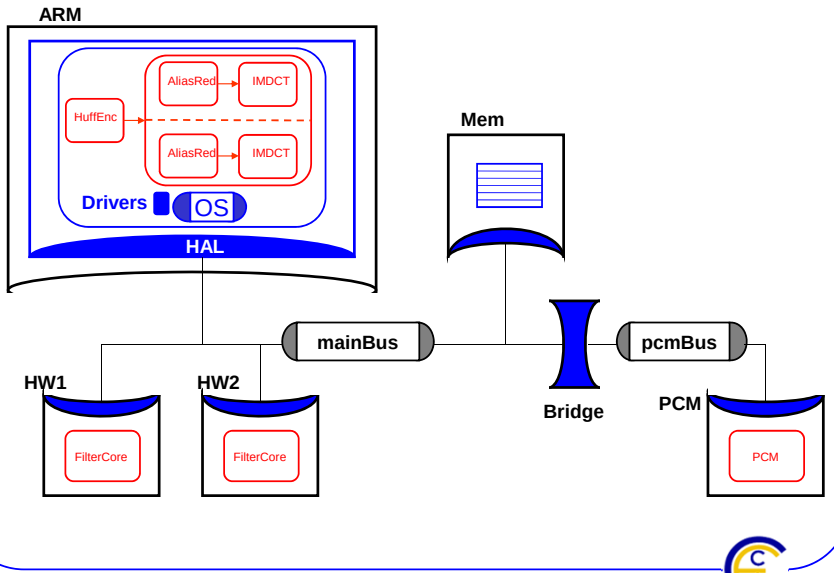
- **Look for parallelism in process hierarchy**
  - *FilterCore* processes are running in parallel
    → Use two identical custom HWs

System Modifications

- **Add two more PEs: HW1 and HW2**
- **Connect HW1 and HW2 to the mainBus**
- **Move processes from ARM to HWs**
  - Channels are automatically inserted

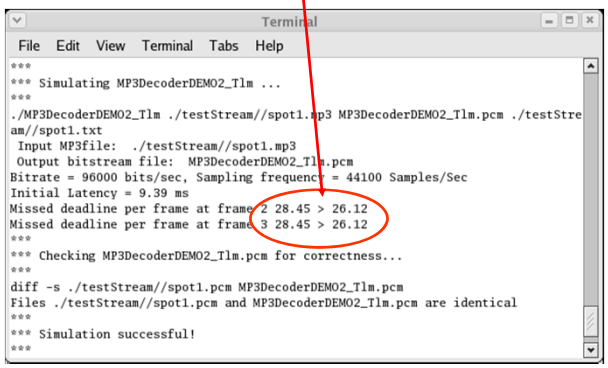


Modified TLM



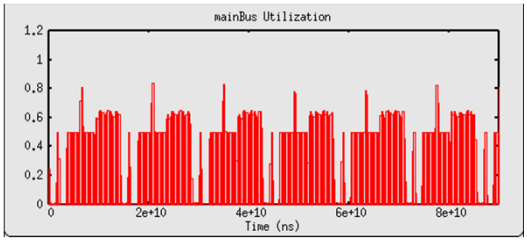
Modified TLM Simulation

- **Simulation of TLM**
  - Functionally correct
  - Frame delay still violates timing constraint

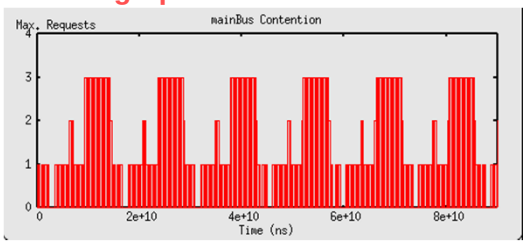


Communication Analysis

- Bus utilization graph

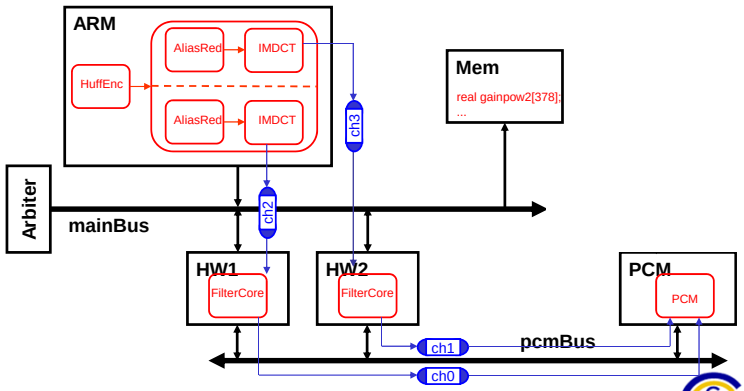


- Bus contention graph

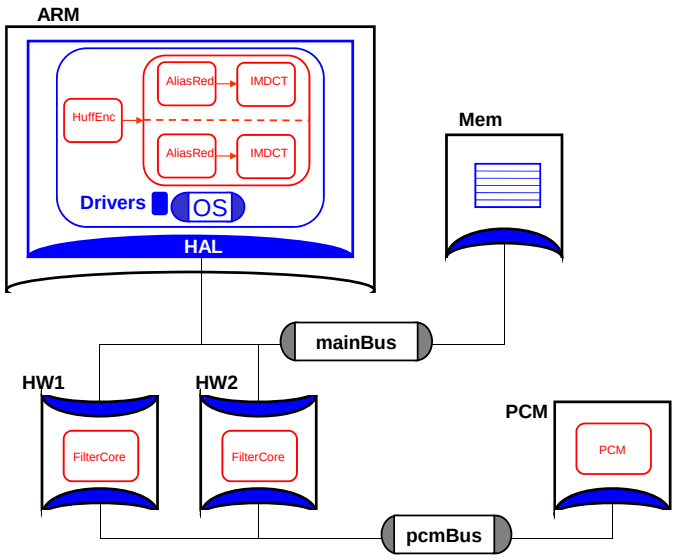


More System Modifications

- Make two ports in HW1, HW2
- Connect HWs directly to the DHS bus
- Remove the bridge



Modified TLM



Modified TLM Simulation

- **Simulation of TLM**
  - Functionally correct
  - Frame delay now meets timing constraint