EECS 222C: System-on-Chip Software Synthesis Lecture 8

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Lecture 8: Overview

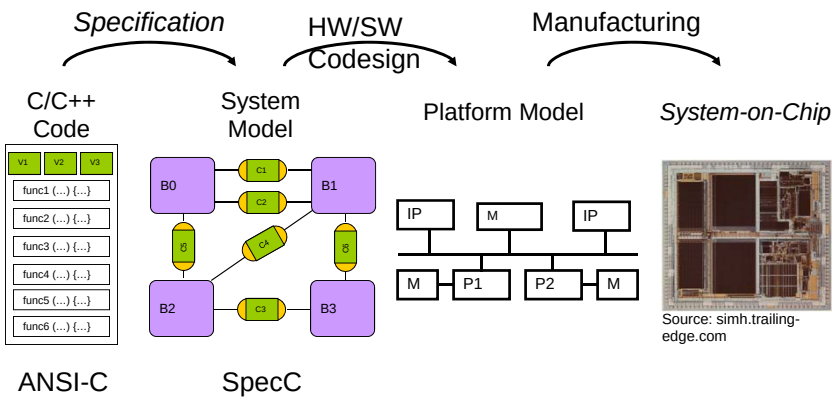
- Assignment 6
  - Discussion
- SoC Design Flow
  - Project Status
- Embedded Software Generation
  - Guest Lecture by Gunar Schirner, 2008
  - "*Systematic Generation of Embedded Software from High-level Models*"
- Assignment 7

Assignment 6

1. Refinement of the MP3 Decoder model in SCE
   - Continue from "Spec" model of previous assignment
   - Select an appropriate system architecture
     - 1 ARM_7TDMI or LEON3 CPU at 50 MHz
     - 0-6 HW_Standard accellerators at 100 MHz
   - Perform the following refinement steps
     - Architecture Refinement
     - Scheduling Refinement
     - Network Refinement
     - Communication Link Refinement
       - Transaction-level model (TLM)
       - Pin-accurate model (PAM)
     - Reference instructions:
       - **`/home/doemer/EECS222C/Assignment6.txt`**
   - Deliverable:
     - Text file "**`refinement.txt`**" with
       - short description of the chosen target architecture
       - simulated execution times of each model
   - Due:
     - by Friday, Nov 12, 2010, at noon
     - by email to **doemer@uci.edu**, with subject "EECS222C HW6"

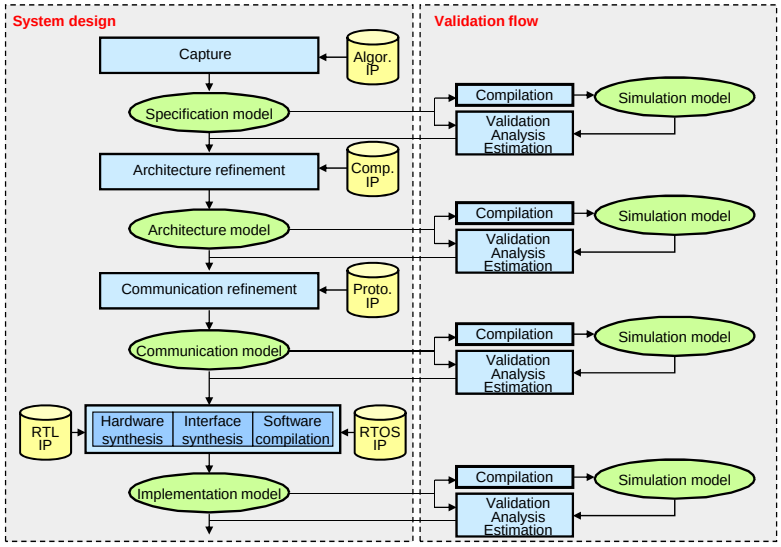
System-on-Chip Co-Design Flow

- MP3 Decoder Project Status:
  - Given: Reference source code (**`mad_C.tar.gz`**)
  - Analyzed: Specification Model (**`mad_SpecC.tar.gz`**)
  - Next: Platform Model with integrated ISS



Source: simh.trailing-edge.com

Refinement-based System Design Flow



Guest Lecture 2008

- ***"Systematic Generation of Embedded Software from High-level Models"***
- Speaker:
  - **Gunar Schirner**
    Center of Embedded Computer Systems, UC Irvine
- Abstract:
  - This talk presents a systematic approach to automatically generate embedded software from an abstract system model. The software generation encompasses RTOS-based multi-tasking, driver generation for external and internal communication, and assembly of the final target binary. The presentation will conclude with a live demonstration that synthesizes embedded software for an example from the automotive domain.
- **`Lecture8-GS-SWgen.pdf`**

Assignment 7

1. SW Synthesis and ISS Integration of the MP3 Decoder in SCE
   - Continue from “TLM” and “PAM” models of previous assignment
   - Perform C code generation
     - Software Synthesis Refinement, C code generation
   - Perform Instruction Set Simulation
     - Software Synthesis Refinement, ISS integration
   - Reference instructions:
     - **`/home/doemer/EECS222C/Assignment7.txt`**
   - Deliverable:
     - Text file “**`SWgen.txt`**” with
       - short (!) description of “your story”
       - execution time of your ISS model
   - Due:
     - by Friday, Nov 19, 2010, at noon
     - by email to **doemer@uci.edu**, with subject “EECS222C HW7”