EECS 222C: System-on-Chip Software Synthesis Lecture 8

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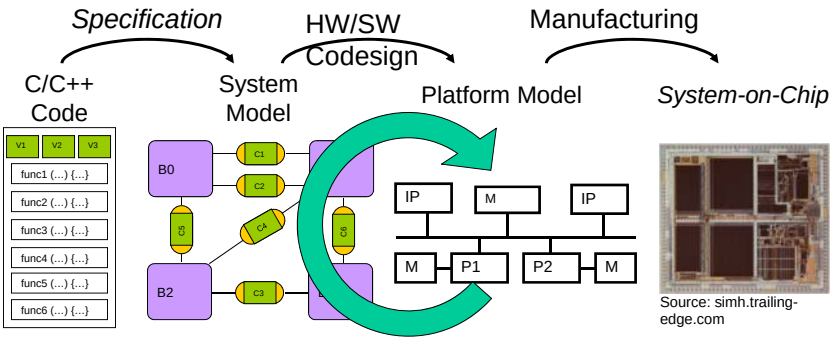
Lecture 8: Overview

- SoC Design Flow
  - Project Status
- Assignment 6
  - Discussion
- Assignment 7
- Embedded Software Generation
  - Guest Lecture by Gunar Schirner, 2008
  - "*Systematic Generation of Embedded Software from High-level Models*"

System-on-Chip Co-Design Flow

- Application Case Study, Project Status:
  - Given: Reference source code (**`mad_C.tar.gz`**)
  - Analyzed: System Model (**`mad_SpecC.tar.gz`**)
  - Refined: Platform Model with integrated ISS
  - Next: System design cycle(s) to meet timing
  - Finally: Hand-off to manufacturing…



Source: simh.trailing-edge.com

Assignment 6

- Evaluate ARM7TDMI as a potential Processor for a SW-only Implementation of the MP3 Decoder
  - Continue from the “Spec” model of the previous assignment
  - Allocate an ARM_7TDMI processor for the entire decoder
    - Choose default port configuration (i.e. 20000ps bus cycle)
    - Choose 50 MHz (change it from default 100MHz)
  - Estimate the execution time and calculate the frame delay
  - Perform the following refinement steps
    - Architecture Refinement
    - Scheduling Refinement
    - Network Refinement
    - Communication Refinement
      - Transaction-level model (TLM)
        - » Code generation: TLM_C model
      - Pin-accurate model (PAM)
        - » Instruction Set Simulator (ISS) model
  - Details: **`/home/eecs222/EECS222C_S13/Assignment6.txt`**

Assignment 6

- Evaluate ARM7TDMI as a potential Processor for a SW-only Implementation of the MP3 Decoder
  - Fill the following table with the estimated/simulated frame delays

Refinement Step	Model	Decode time per frame
Profiling estimation	Spec	
Architecture Refinement	Arm7Arch	
Scheduling Refinement	Arm7Sched	
Network Refinement	Arm7Net	
Transaction-Level Refinement	Arm7TLM	
C Code Generation	Arm7TLM_C	
Pin-Accurate Refinement	Arm7PAM	
Instruction Set Simulation	Arm7ISS	

  - Submit as file: **`hw6/ARM7_Evaluation.pdf`**

Assignment 6

- Discussion
  - Test bench improvements
    - Stimulus: calls exit!? Should not!
    - Monitor: should quit the simulation and report the total time!
    - Simulation: Pass the number of frames (**8**) as 3rd argument
  - Corrections to compilation settings
    - Assertions are part of the DUT!? Must not!
    - Turn assertions (and debug) off: pass **–DNDEBUG** to compiler
  - Reported ISS cycles vs. reported decoding time!?
    - ISS model in SCE version 2010 has a bug: processor speed is fixed to 100Mhz!
    - Switch to "latest" SCE version 2012+ (**`/opt/sce/bin/setup.csh`**)
  - Profiling estimation is inaccurate!
    - Several times too optimistic for the ARM7
    - Calibrate profiler weight tables by corresponding factor

Assignment 7

- Re-evaluate ARM7TDMI as a potential Processor for a SW-plus-HW Implementation of the MP3 Decoder
  - Allocate an ARM_7TDMI processor for the software
    - Choose desired clock period (change it from default 10000ps)
  - Allocate up to 6 custom HW units for acceleration
    - Keep default clock frequency of 100 MHz
  - Perform the system design refinement steps
    - Architecture Refinement
    - Scheduling Refinement
    - Network Refinement
    - Communication Refinement
      - Transaction-level model (TLM)
        - » Code generation: TLM_C model
      - Pin-accurate model (PAM)
        - » Instruction Set Simulator (ISS) model
  - Details: **`/home/eecs222/EECS222C_S13/Assignment7.txt`**

Assignment 7

- Re-evaluate ARM7TDMI as a potential Processor for a SW-plus-HW Implementation of the MP3 Decoder
  - Fill the following table with the estimated/simulated frame delays

Refinement Step	Model	Decode time per frame
Profiling estimation	Spec	
Architecture Refinement	Arch	
Scheduling Refinement	Sched	
Network Refinement	Net	
Transaction-Level Refinement	TLM	
C Code Generation	TLM_C	
Pin-Accurate Refinement	PAM	
Instruction Set Simulation	ISS	

  - Submit as file: **`hw7/ARM7plusHW_Evaluation.pdf`**
  - Submit also the final ISS model: **`hw7/ISS.sir`**

Guest Lecture 2008

- ***"Systematic Generation of Embedded Software from High-level Models"***
- Speaker:
  - **Gunar Schirner**
    Center of Embedded Computer Systems, UC Irvine
- Abstract:
  - This talk presents a systematic approach to automatically generate embedded software from an abstract system model. The software generation encompasses RTOS-based multi-tasking, driver generation for external and internal communication, and assembly of the final target binary. The presentation will conclude with a live demonstration that synthesizes embedded software for an example from the automotive domain.
- **`Lecture8-GS-SWgen.pdf`**