EECS 222C: System-on-Chip Software Synthesis Lecture 9

Rainer Dömer

doemer@uci.edu

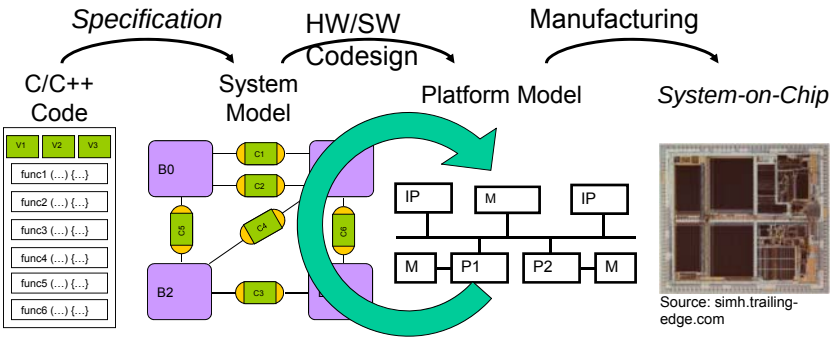
The Henry Samueli School of Engineering
Electrical Engineering and Computer Science
University of California, Irvine

Lecture 9: Overview

- SoC Design Flow
  - Project status, completion
- Assignment 7
  - Discussion
- Embedded Software
  - Scheduling algorithms
    - Periodic scheduling
      - RMS, EDF
    - Priority inversion
      - Mars Pathfinder Example

System-on-Chip Co-Design Flow

- Application Case Study, Project Status:
  - Given: Reference source code (**`mad_C.tar.gz`**)
  - Analyzed: System Model (**`mad_SpecC.tar.gz`**)
  - Refined: Platform Model with integrated ISS
  - Next: System design cycle(s) to meet timing
  - Finally: Hand-off to manufacturing…



Source: simh.trailing-edge.com

Assignment 7

- Re-evaluate ARM7TDMI as a potential Processor for a SW-plus-HW Implementation of the MP3 Decoder
  - Allocate an ARM_7TDMI processor for the software
    - Choose desired clock period (change it from default 10000ps)
  - Allocate up to 6 custom HW units for acceleration
    - Keep default clock frequency of 100 MHz
  - Perform the system design refinement steps
    - Architecture Refinement
    - Scheduling Refinement
    - Network Refinement
    - Communication Refinement
      - Transaction-level model (TLM)
        - » Code generation: TLM_C model
      - Pin-accurate model (PAM)
        - » Instruction Set Simulator (ISS) model
  - Details: **`/home/eecs222/EECS222C_S13/Assignment7.txt`**

Assignment 7

- Re-evaluate ARM7TDMI as a potential Processor for a SW-plus-HW Implementation of the MP3 Decoder
  - Fill the following table with the estimated/simulated frame delays

Refinement Step	Model	Decode time per frame
Profiling estimation	Spec	
Architecture Refinement	Arch	
Scheduling Refinement	Sched	
Network Refinement	Net	
Transaction-Level Refinement	TLM	
C Code Generation	TLM_C	
Pin-Accurate Refinement	PAM	
Instruction Set Simulation	ISS	

  - Submit as file: **`hw7/ARM7plusHW_Evaluation.pdf`**
  - Submit also the final ISS model: **`hw7/ISS.sir`**

Assignment 7: Problem Solving…

1. Slow server response and simulator run time
   - Symptoms:
     - Shell commands respond very slowly
     - Simulator runs unreasonably slow (e.g. more than a minute for models above TLM)
   - Analysis:
     - Shared server may be overloaded due to too many users and/or jobs
   - Possible Solutions:
     - Monitor the server load!
     - Use **`uptime`** and/or **`top`** commands
     - Login to server with lowest load
       - **`gamma:   ..., 14 users,  load average: 14.08, 13.47, 11.92`**
       - **`omicron: ...,  0 users,  load average: 0.04, 0.02, 0.00`**
       - **`iota:    ..., 10 users,  load average: 0.00, 0.02, 0.00`**

Assignment 7: Problem Solving…

2. Large frame delay in ISS model
   - Symptom:
     - Simulation of TLM/PAM models estimated frame delays such as **`Decode time per frame = 24.282 ms`**
     - Simulation of ISS model reports frame delays such as **`Decode time per frame = 64.174 ms`**
   - Analysis:
     - TLM/PAM computation time is only estimated (by SCE profiler)
     - Profiling produces only *fidelity* (not absolute *accuracy*!)
     - Profiling weight tables for ARM7 assume very optimistic cycles
       - Assumptions include zero cache-misses, pipeline stalls, etc.
   - Possible Solutions:
     - Trust the ISS, not the profiler!
     - Calibrate the weight tables at allocation by a factor (e.g. 64.174 / 24.282 ≈ 2.6x)

Assignment 7: Problem Solving…

3. Communication times can be very slow
   - Symptom:
     - Simulation shows that delay per frame increases drastically in TLM and PAM models
   - Analysis:
     - Communication time is not taken into account before
     - TLM and PAM include accurate communication delay
     - Communication can be a bottleneck for certain architectures
       - Congestion due to single bus and/or high traffic
       - Indirect communication from slave to slave via master
   - Potential Solutions:
     - Review bus network by viewing connectivity in Network model
     - Introduce a separate bus between hardware components
       - See **`Lecture7-ASPDAC07-AG-MP3.pdf`**
     - Increase bus frequency

Assignment 7: Problem Solving…

4. Incorrect network setup
   - Symptoms:
     - ERROR #5535: Channel instance 'ar_cc__xr0__HW1__HW2' connects two PEs (HW1 and HW2) not reachable with given conectivity
     - ERROR #5533: Channel instance 'ar_cc__ar_tid_III_decode__ARM7__HW1' is not connected to only one PE, which is not allowed by network refinement
   - Analysis:
     - Network refinement fails to map channels to specified network
     - Network specification needs revision
   - Potential Solutions:
     - Ensure channel routing is possible (path exists)
     - Ensure master/slave relationship is obeyed
     - Ensure all behaviors involved are isolated

Assignment 7: Problem Solving…

5. IS Simulation is stuck
   - Symptoms:
     - PAM model simulates fine
     - Derived ISS model runs but shows no progress even after an hour
   - Analysis:
     - Difficult to diagnose without more data (needs code inspection, instrumentation, debugging)
     - Likely communication between CPU and slaves fails
   - Potential Solutions:
     - Ensure slaves listen to correct addresses
     - ➢ For the AMBA bus in SCE, slave1 listens to 0x1xxx xxxx, slave 2 listens to 0x2xxx xxxx, and so on
     - Ensure scheduling (execution order) across PEs matches (e.g. master sends X but slave waits for Y results in deadlock)

Assignment 8

- ARM7-plus-HW Implementation of the MP3 Decoder
  that meets the real-time requirement
  and minimizes HW resources and power
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  that meets the real-time requirement
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Pin-Accurate Refinement	PAM	
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Embedded Software

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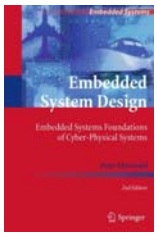
    - RMS, EDF
  - Priority inversion
    - Mars Pathfinder Example



➢ Excerpts from Chapters 6.3 and 4.1 in
  - *"Embedded System Design"*
    Embedded Systems Foundations
    of Cyber-Physical Systems
    by P. Marwedel,
    2nd edition, Springer, 2011.
    - ➢ **`Lecture9-subset-es-marw-6.3-periodic.pdf`**
    - ➢ **`Lecture9-subset-es-marw-4.1-rtos.pdf`**