

ECPS 203

Embedded Systems Modeling and Design

Lecture 14

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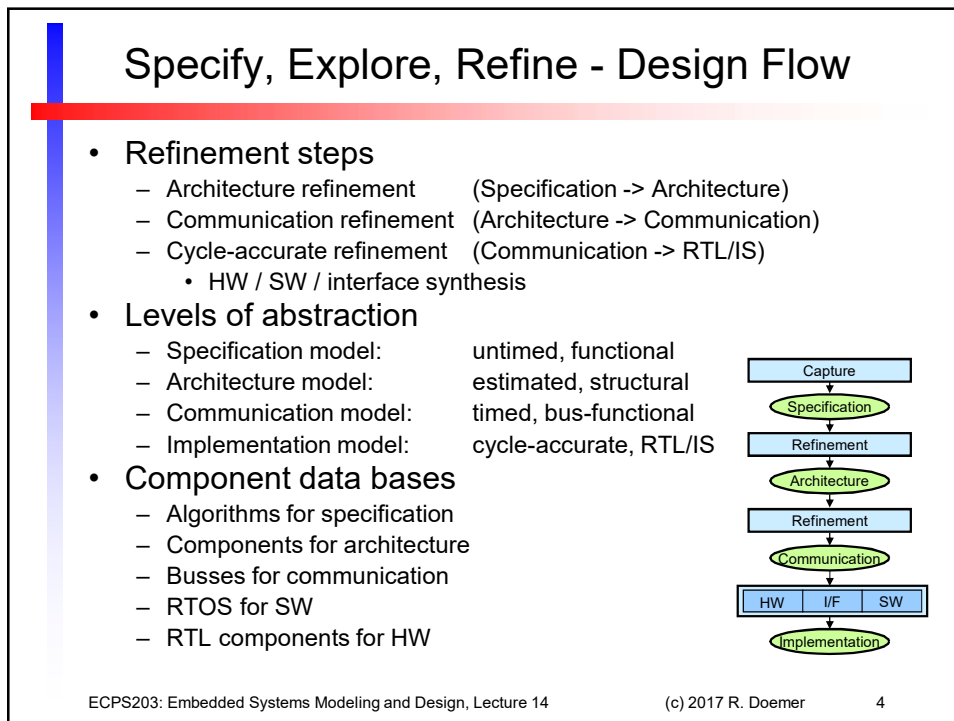
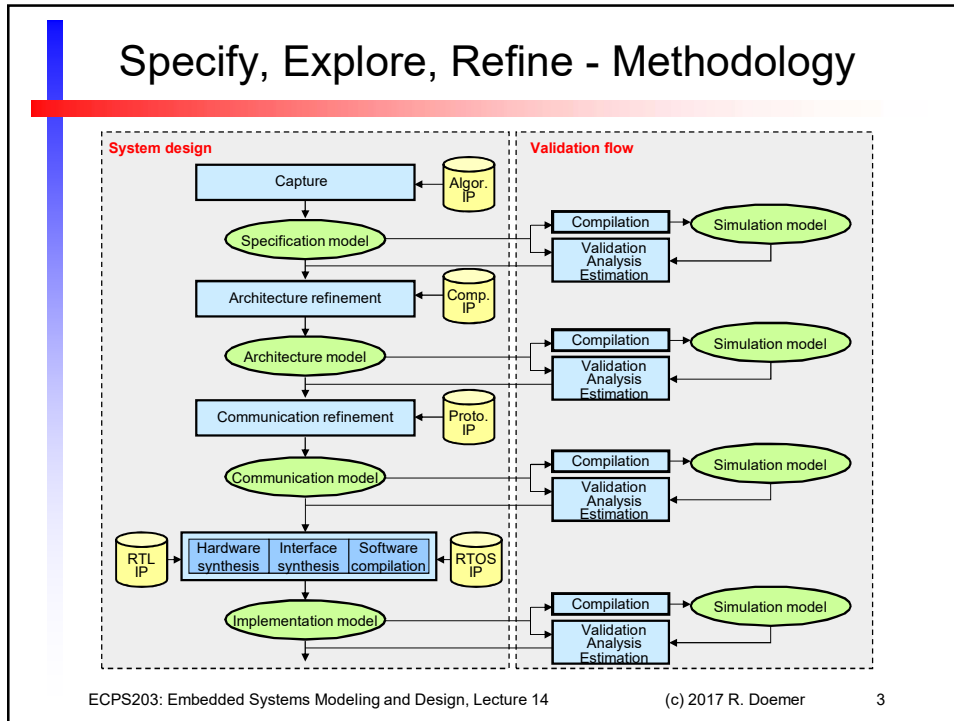
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Lecture 14: Overview

- Embedded System Design Flow
 - Refinement-based design flow
 - Specify
 - Explore
 - Refine
- System-on-Chip Environment (SCE)
 - Application example: GSM Vocoder
 - Interactive demonstration (part 2)



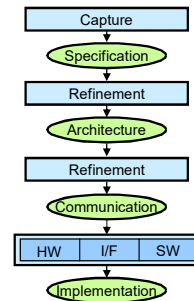
Specify, Explore, Refine - Design Flow

- Refinement Step 1: System Architecture

- Allocation of Processing Elements (PE)
 - Type and number of processors
 - Type and number of custom hardware blocks
 - Type and number of system memories
- Mapping to PEs
 - Map each behavior to a PE
 - Map each channel to a PE
 - Map each variable to a PE

- Result

- System architecture of concurrent PEs with abstract communication via channels



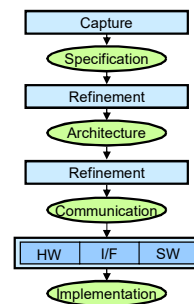
Specify, Explore, Refine - Design Flow

- Refinement Step 2: PE Scheduling

- For each PE, serialize the execution of behaviors to a single thread of control
- Option (a): Static scheduling
 - For each set of concurrent behaviors, determine fixed order of execution
- Option (b): Dynamic RTOS scheduling
 - Choose scheduling policy, e.g. round-robin or priority-based
 - For each set of concurrent behaviors, determine scheduling priority

- Result

- System model with abstract scheduler inserted in each PE



Refinement-based System Design Flow

- Step 3: Network / Communication Refinement
 - Allocation of system busses
 - Type and number of system busses
 - Type of bus protocol for each bus (if applicable)
 - Number of transducers (if applicable)
 - System connectivity
 - Mapping of channels to busses
 - Map each channel to a system bus (or a network of multiple busses)
 - Result
 - Transaction-Level Model (TLM), or Bus-Functional Model (BFM)

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Refinement-based System Design Flow

- Step 4: Hardware Refinement (for HW PE)
 - Allocation of Register Transfer Level (RTL) components
 - Type and number of functional units (e.g. adder, multiplier, ALU)
 - Type and number of storage units (e.g. registers, register files)
 - Type and number of interconnecting busses (drivers, multiplexers)
 - Scheduling
 - Basic blocks assigned to super-states
 - Individual operations assigned to clock cycles
 - Binding
 - Bind functional operations to functional units
 - Bind variables to storage units
 - Bind assignments/transfers to busses
 - Result
 - Clock-cycle accurate model of each HW PE
 - Output: Synthesizable Verilog description

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Refinement-based System Design Flow

- Step 5: Software Refinement (for SW PE)
 - C code generation
 - For selected target processor
 - RTOS targeting
 - Thin adapter layer for selected target RTOS
 - Cross-compilation to Instruction Set Architecture
 - for Instruction Set Simulation (ISS)
 - for target processor embedded in target system
 - Assembly and Linking
 - Result
 - Clock-cycle accurate, or instruction-accurate model of each SW PE
 - Output: binary image

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graph TD
    Capture[Capture] --> Specification([Specification])
    Specification --> Refinement1[Refinement]
    Refinement1 --> Architecture([Architecture])
    Architecture --> Refinement2[Refinement]
    Refinement2 --> Communication([Communication])
    Communication --> HW_IF_SW[HW | I/F | SW]
    HW_IF_SW --> Implementation([Implementation])
    
```

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SCE Demonstration

- Application Example: GSM Vocoder
 - Enhanced full-rate voice codec
 - GSM standard for mobile telephony (GSM 06.10)
 - Lossy voice encoding/decoding
 - Incoming speech samples @ 104 kbit/s
 - Encoded bit stream @ 12.2 kbit/s
 - Frames of $4 \times 40 = 160$ samples ($4 \times 5\text{ms} = 20\text{ms}$ of speech)
 - Real-time constraint:
 - max. 20ms per speech frame
(max. total of 3.26s for sample speech file)
 - SpecC specification model
 - 29 hierarchical behaviors (9 par, 10 seq, 10 fsm)
 - 73 leaf behaviors
 - 9139 formatted lines of SpecC code
(~13000 lines of original C code, including comments)

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