





















Project Assignment 8						
 Pipelined and parallel model of the Canny Edge Detector Back-annotation of measured timing delays 4-way parallelization of BlurX and BlurY modules (step 5) 						
Receive, Make_Kernel BlurX 17 BlurY 18 Derivative_X_Y 4 Magnitude_X_Y 10 Non_Max_Supp 8 Apply_Hysteresis 6 TOTAL: 65 = Throughput: 1/	0 10 20 80 30 30 70 40 40	ms ms ms ms ms ms ms ms 20ms	427 455 480 1030 830 670 ==== 3892 ====) ms / ms 5 ms) ms) ms) ms) ms 2 ms 		
0.549 FPS ECPS203: Embedded Systems Modeling and Design, Lecture 19				1 FPS 8 R. Doemer	32	

