

# ECPS 203

## Embedded Systems Modeling and Design

### Lecture 2

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## Lecture 2: Overview

- Embedded System Design
  - Complexity Challenges
  - Abstraction Levels
  - Top-down Design Flow
- Abstract Modeling of Embedded Systems
  - Models of Computation
  - System-Level Description Languages
- Separation of Concerns
  - Computation vs. Communication

## Embedded System Design

- Embedded System in CPS context
  - Software
  - Hardware
- Design Challenges
  - Hardware design gap
  - Software design gap
  - System design gap

The diagram shows a Cyber-Physical System (CPS) block. Inside, there are three main components: Sensors on the left, Actuators on the right, and an Embedded Computer System in the center. The Embedded Computer System is further divided into Software (green) and Hardware (blue). A large grey arrow labeled 'Control' loops around the Embedded Computer System, indicating a feedback loop between the sensors and actuators through the computer system.

The graph plots four variables against an unlabeled horizontal axis. Moore's Law is shown as a blue line with a moderate positive slope. The System Gap is a black line with a steep positive slope. The HW Gap is a blue line with a shallower positive slope. The SW Gap is a red line with a very shallow positive slope. All lines originate from the origin and trend upwards.

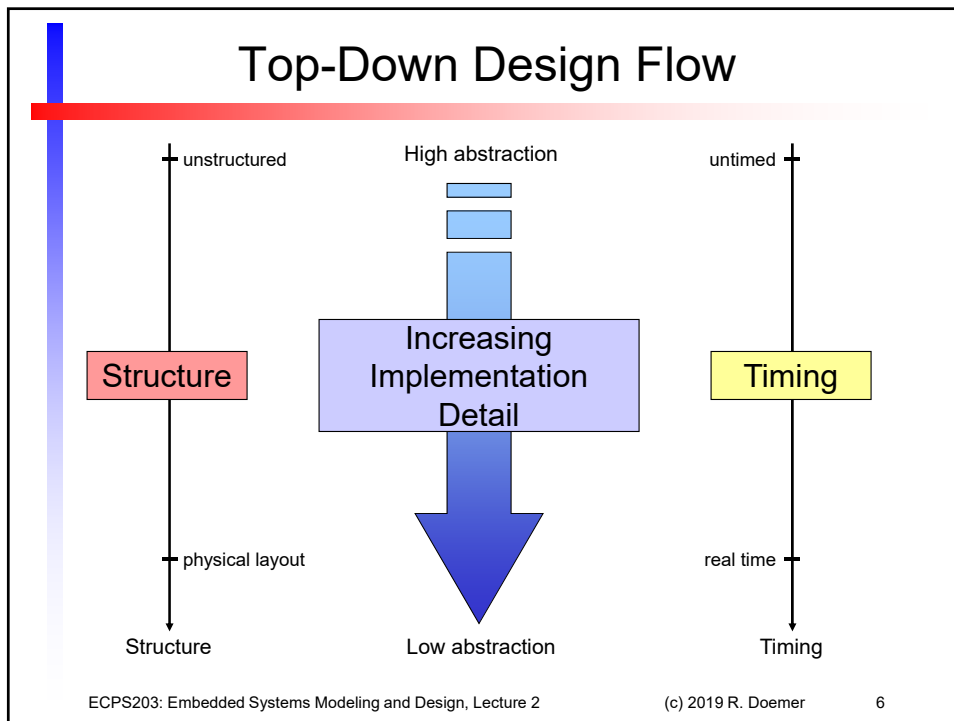
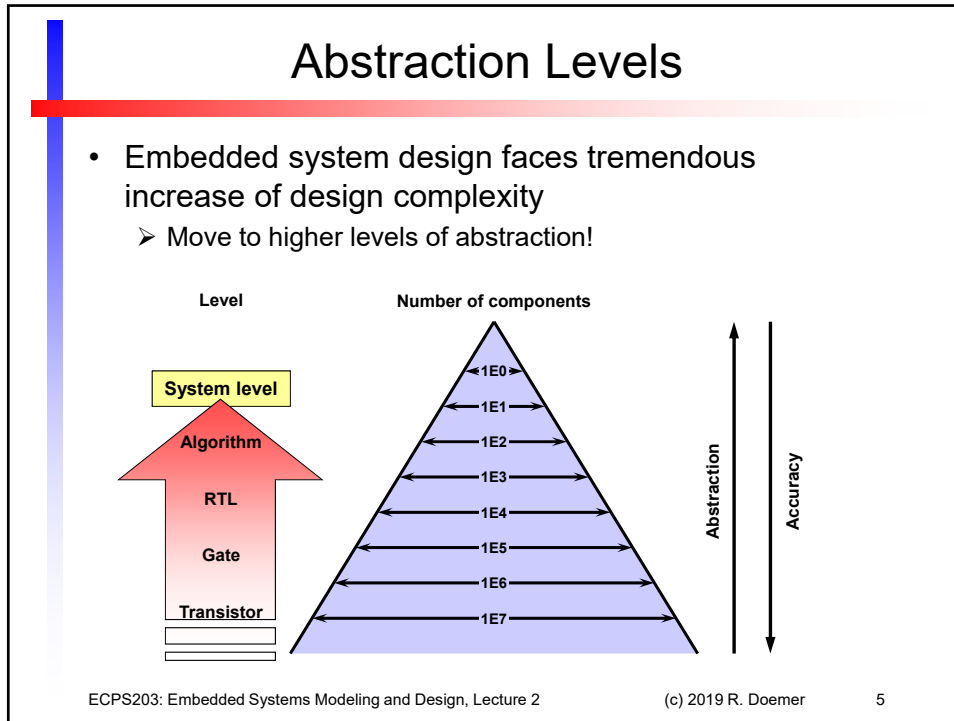
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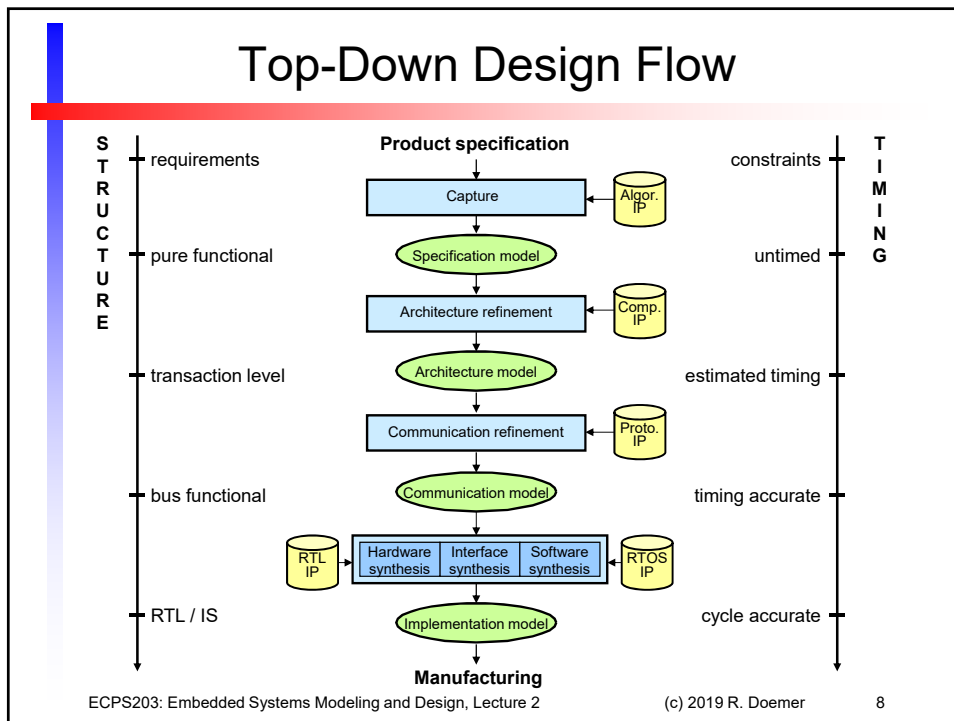
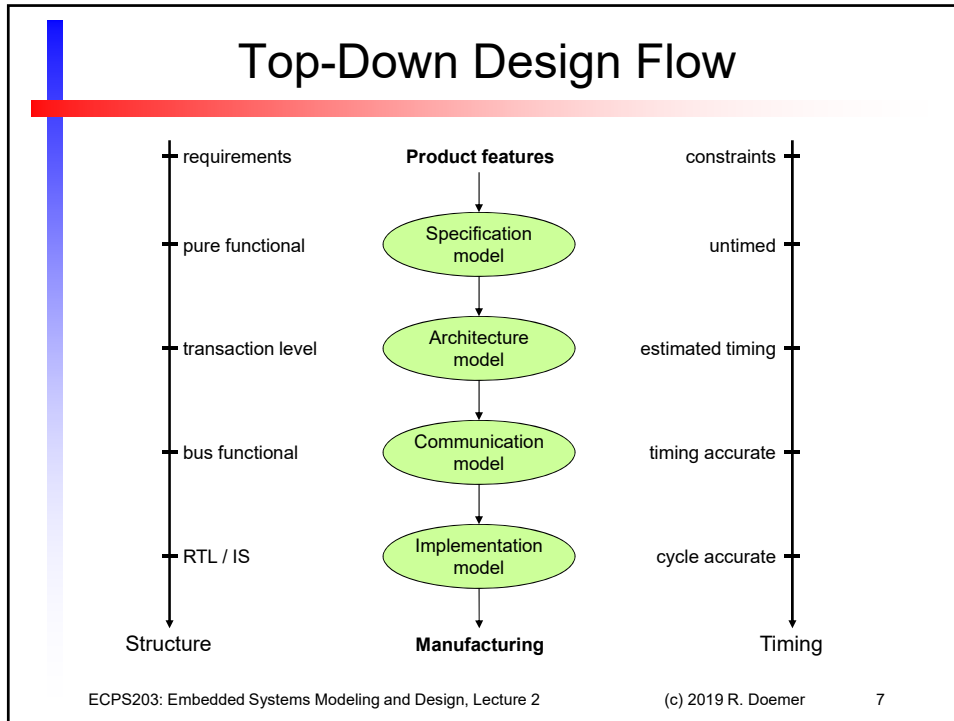
## Abstraction Levels

- Embedded system design faces tremendous increase in design complexity

The diagram is a pyramid with seven horizontal levels. From top to bottom, the levels are: System, Algorithm, RTL, Gate, and Transistor. The number of components at each level is indicated by a double-headed arrow across the width of the pyramid: 1E0 for System, 1E1 for Algorithm, 1E2 for RTL, 1E3 for Gate, 1E4 for Transistor, 1E5 for Gate, 1E6 for Transistor, and 1E7 for Transistor. To the right of the pyramid, two vertical arrows indicate the direction of change: an upward arrow labeled 'Abstraction' and a downward arrow labeled 'Accuracy'.

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## Abstract Modeling

- Model of Computation
  - Formal description of a system model at high abstraction level
    - Specification
    - Documentation
    - Reasoning
    - Validation
    - Synthesis
- Models for Hardware and Software design
  - State-based models of computation
    - from Finite State Machine (FSM)
    - to Program State Machine (PSM)

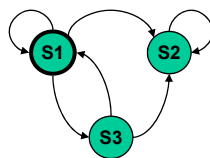
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## Models of Computation

- Finite State Machine (FSM)
  - Basic model for describing control
  - States and state transitions
    - $FSM = \langle S, I, O, f, h \rangle$
  - Two types:
    - Mealy-type FSM (input-based)
    - Moore-type FSM (state-based)



FSM model

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## Models of Computation

- Finite State Machine (FSM)
- Data Flow Graph (DFG)
  - Basic model for describing computation
  - Directed graph (acyclic)
    - Nodes: operations
    - Edges: data flow, dependency of operations

DFG model

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## Models of Computation

- Finite State Machine (FSM)
- Data Flow Graph (DFG)
- Finite State Machine with Data (FSMD)
  - Combined model for control and computation
    - FSMD = FSM + DFG
  - Implementation: controller plus data path (RTL processor)

FSMD model

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## Models of Computation

- Finite State Machine (FSM)
- Data Flow Graph (DFG)
- Finite State Machine with Data (FSMD)
- Super-State FSM with Data (SFSMD)
  - FSMD with complex, multi-cycle states
    - States described by procedures in a programming language

```
a = a + b;
c = c + d;
```

```
a = 42;
while (a < 100)
{
  b = b + a;
  if (b > 50)
    c = c + d;
  a = a + c;
}
```

SFSMD model

```
a = 42;
b = a * 2;
for (c=0; c<100; c++)
{
  b = c + a;
  if (b < 0)
    b = -b;
  else
    b = b + 1;
  a = b * 10;
}
```

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## Models of Computation

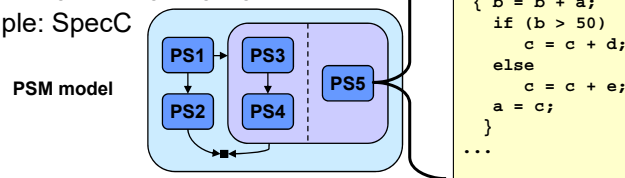
- Finite State Machine (FSM)
- Data Flow Graph (DFG)
- Finite State Machine with Data (FSMD)
- Super-State FSM with Data (SFSMD)
- Hierarchical Concurrent FSM (HCFSM)
  - FSM extended with hierarchy and concurrency
    - Multiple FSMs composed hierarchically and in parallel
  - Example: Statecharts

HCFSM model

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## Models of Computation

- Finite State Machine (FSM)
- Data Flow Graph (DFG)
- Finite State Machine with Data (FSMD)
- Super-State FSM with Data (SFSMD)
- Hierarchical Concurrent FSM (HCFSM)
- Program State Machine (PSM)
  - HCFSM plus programming language
    - States described by procedures in a programming language
  - Example: SpecC



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## System-Level Description Languages

- Goals and Requirements
  - Formality
    - Formal syntax and semantics
  - Executability
    - Validation through simulation
  - Synthesizability
    - Implementation in HW and/or SW
    - Support for IP reuse
  - Modularity
    - Hierarchical composition
    - Separation of concepts
  - Completeness
    - Support for all concepts found in embedded systems
  - Orthogonality
    - Orthogonal constructs for orthogonal concepts
  - Simplicity
    - Minimality

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## System-Level Description Languages

- Requirements supported by existing languages

	C	C++	Java	VHDL	Verilog	HardwareC	Statecharts	SpecCharts	SpecC
Behavioral hierarchy	○	○	○	○	○	○	○	●	●
Structural hierarchy	○	○	○	○	●	●	●	○	○
Concurrency	○	○	◐	●	●	●	●	●	●
Synchronization	○	○	◐	●	●	●	●	●	●
Exception handling	◐	●	●	○	○	○	○	◐	●
Timing	○	○	○	○	●	●	◐	◐	◐
State transitions	○	○	○	○	○	○	○	●	●
Composite data types	●	●	●	●	●	◐	○	○	●

○ not supported      ◐ partially supported      ● supported

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- Requirements supported by existing languages

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Behavioral hierarchy	○	○	○	○	○	○	○	●	●	○
Structural hierarchy	○	○	○	○	●	●	●	○	○	●
Concurrency	○	○	◐	●	●	●	●	●	●	●
Synchronization	○	○	◐	●	●	●	●	●	●	●
Exception handling	◐	●	●	○	○	○	○	◐	●	○
Timing	○	○	○	○	●	●	◐	◐	◐	●
State transitions	○	○	○	○	○	○	○	●	●	○
Composite data types	●	●	●	●	●	◐	○	○	●	●

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## System-Level Description Languages

- Examples of Languages in Use Today

- C/C++
  - ANSI standard programming languages, software design
  - Initially used for system design because of availability, practicality
- SystemC
  - IEEE standard 1666-2011 (initially created at UCI, standardized by OSCI)
  - C++ library and application programming interface (API)
- SpecC
  - SLDL with compiler, based on the ANSI C language standard
  - Designed and built at UCI, promoted by SpecC Technology Open Consortium
- Matlab
  - Algorithm design, specification and simulation in engineering
- UML
  - Unified Modeling Language, graphical software specification and engineering
- SystemVerilog
  - Verilog with C extensions
- SDL
  - Telecommunication standard by ITU, used in COSMOS

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## System-Level Description Languages

- Examples of Languages in Use Today, **Course Coverage**

- C/C++
  - ANSI standard programming languages, software design
  - Initially used for system design because of availability, practicality
- **SystemC**
  - IEEE standard 1666-2011 (initially created at UCI, standardized by OSCI)
  - C++ library and application programming interface (API)
- **SpecC (concepts!)**
  - SLDL with compiler, based on the ANSI C language standard
  - Designed and built at UCI, promoted by SpecC Technology Open Consortium
- Matlab
  - Algorithm design, specification and simulation in engineering
- UML
  - Unified Modeling Language, graphical software specification and engineering
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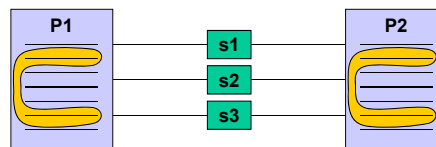
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## Separation of Concerns

- Fundamental Principle in Modeling of Systems
  - *Clear separation of concerns*
    - address separate issues independently
- System-Level Description Language (SLDL)
  - Orthogonal concepts
  - Orthogonal constructs
- System-level Modeling
  - Computation
    - encapsulated in modules / behaviors
  - Communication
    - encapsulated in channels

## Computation vs. Communication

- Traditional model
  - Processes and signals



- VHDL example:

```
entity P1 [...] process [...]
s1 <= '1';
s2 <= '1';
wait until s3'event and s3 = '1';
s2 <= '0';
xy = x + 2 * y;
s1 <= xy;
s2 <= '1';
wait until s3'event and s3 = '1';
s1 <= '0';
s2 <= '0';
[...]
```

- Mixture of computation and communication
  - Automatic replacement impossible!

## Computation vs. Communication

- SpecC model
  - Behaviors and channels
  - SpecC example:
 

```
behavior B1 [...]
{
  c.send(1);

  xy = x + 2 * y;

  c.send(xy);

  v1 = 0;
  [...]
}
```

```
channel C1 [...]
{
  send (int d)
  { v1 = d;
    notify e2;
    wait e3;
  }
  [...]
}
```
- Clear separation of computation and communication
  - Plug-and-play!

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## Computation vs. Communication

- Traditional model
 

P1

P2

  - Processes and signals
  - Mixture of computation and communication
  - Automatic replacement impossible
- SpecC model
 

B1

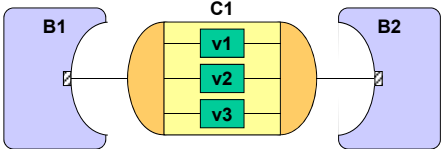
B2

  - Behaviors and channels
  - Separation of computation and communication
  - Plug-and-play

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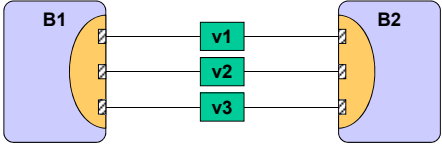
## Computation vs. Communication

- System Model
  - Specification
  - Validation
  - Exploration



- Computation in behaviors
- Communication in channels

- Implementation Model
  - Synthesis
    - e.g. Verilog, VHDL, or SystemC

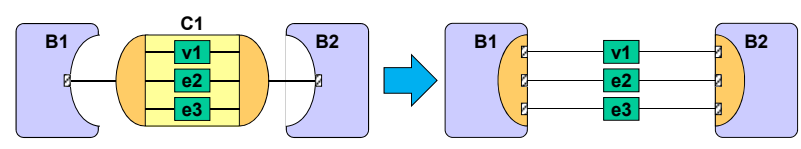


- Channel disappears, signals get exposed
- Communication protocol is *inlined* into behaviors

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## Computation vs. Communication

- Communication Protocol Inlining



– SystemC example:

```
SC_MODULE(M1)
{
  [...]
  c.send(1);

  xy = x + 2 * y;

  c.send(xy);

  v1 = 0;
  [...]
}
```

```
SC_CHANNEL(C1)
{
  [...]
  send(int d)
  {
    v1 = d;
    e2.notify();
    wait(e3);
  }
  [...]
}
```

```
SC_MODULE(M1)
{
  [...]
  v1 = 1;
  e2.notify();
  wait(e3);
  xy = x + 2 * y;
  v1 = xy;
  e2.notify();
  wait(e3);
  v1 = 0;
  [...]
}
```

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