

# ECPS 203

## Embedded Systems Modeling and Design

### Lecture 6

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## Lecture 6: Overview

- SystemC: From the Ground Up (Part 2)
  - Processes and events
  - Channels and interfaces
  - Ports
- Project Discussion
  - Assignment 2
  - Assignment 3

## IEEE SystemC Language

- SystemC: From the Ground Up (Part 2)
  - **DAC15\_systemC\_Training.pdf**, slides 25 through 43 by David Black, Doulos
    - SystemC training day at Design Automation Conference 2015
  - *“The Definitive Guide to SystemC: The SystemC Language”*
  - Core Concepts and Syntax
    - Review: Modules and connectivity
    - Processes and events

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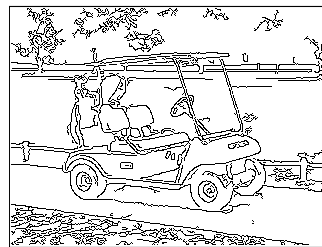
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## ECPS 203 Project

- Application Example: Canny Edge Detector
  - Embedded system model for image processing:  
Automatic edge detection in a digital camera



golfcart.pgm



golfcart.pgm\_s\_0.60\_l\_0.30\_h\_0.80.pgm

- Application source and documentation:
  - John Canny, “A Computational Approach to Edge Detection”, IEEE TPAMI, 1986.
  - [http://en.wikipedia.org/wiki/Canny\\_edge\\_detector](http://en.wikipedia.org/wiki/Canny_edge_detector)
  - [ftp://figment.csee.usf.edu/pub/Edge\\_Comparison/source\\_code/canny.src](ftp://figment.csee.usf.edu/pub/Edge_Comparison/source_code/canny.src)

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## Project Assignment 2

- Task: Clean C++ model with static memory allocation
  - Prepare the C++ source code for modeling in SystemC
  - Configure parameters for specific application
  - Apply static memory allocation
- Steps
  1. Fix the off-by-one bug in the `non_max_supp` function
  2. Clean-up the code for compilation without warnings
  3. Fix configuration parameters to compile-time constants
  4. Remove or replace dynamic memory allocation
- Deliverables
  - Source code and text file: `canny.cpp`, `canny.txt`
- Due
  - Wednesday, October 16, 2019, 6pm

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## Project Assignment 3

- Task: Introduction to SystemC
  - Capture and simulate the introductory example by Doulos
- Steps
  1. Structural model is shown on slide 25
  2. Source file structure is shown on slide 32
  3. Capture the partial source code provided on slides 21-36
  4. Fill in the omitted source code for the monitor module
    - For test cases 1\*6, 2\*6, ..., 7\*6, monitor and validate the output
  5. Simulate the model with Accellera SystemC library
- Deliverables
  - Source files, `Makefile`, `README` in `hw3.tar.gz`
- Due
  - Wednesday, October 23, 2019, 6pm

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