

EECS 222: Embedded System Modeling Lecture 12

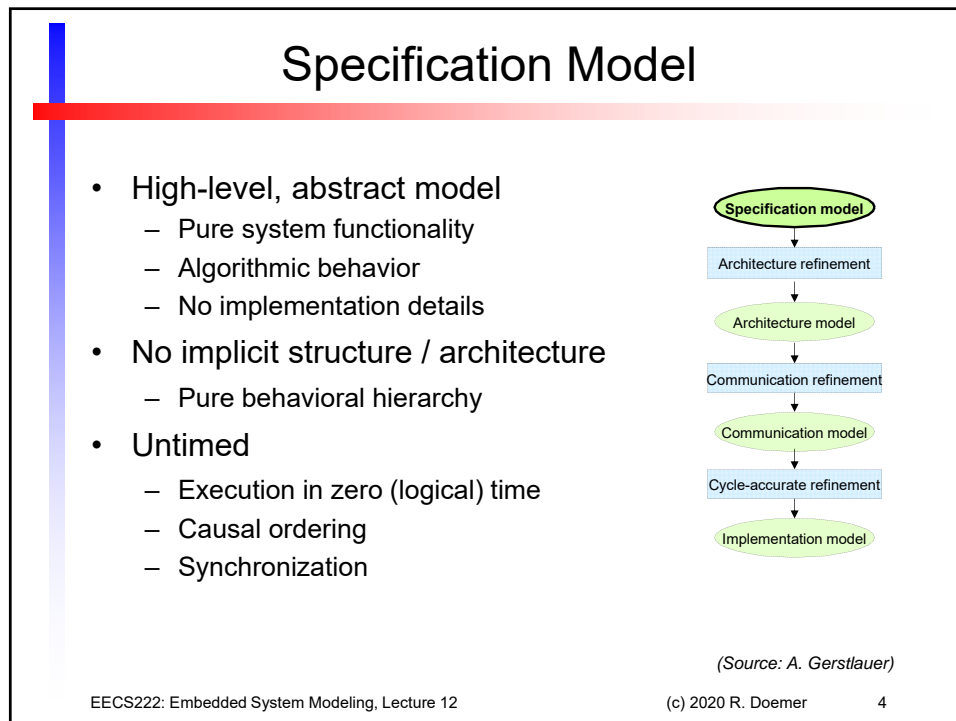
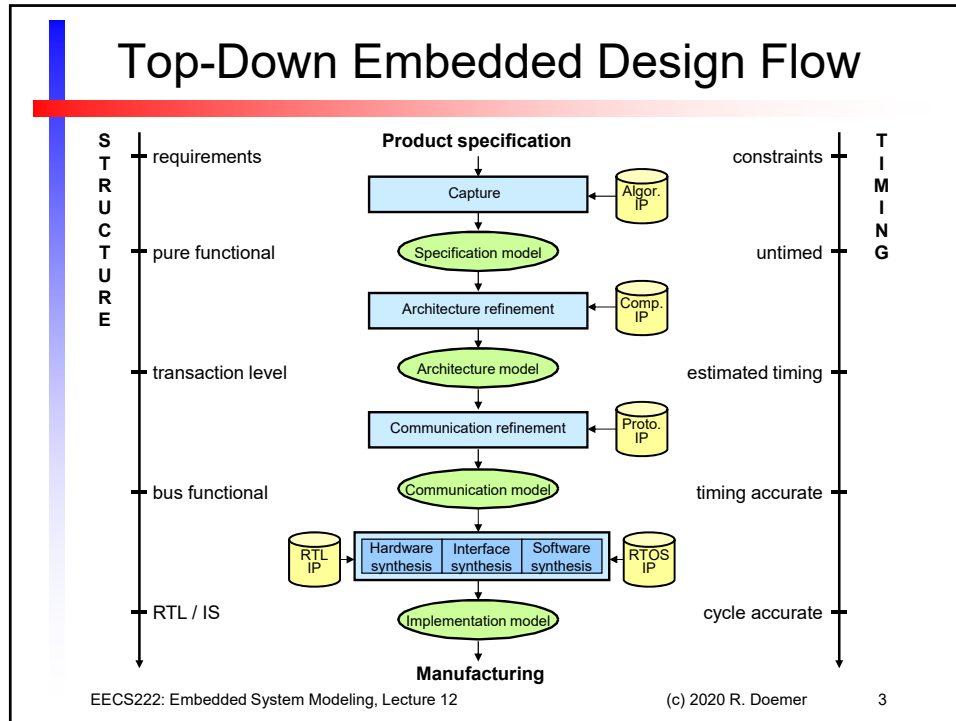
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Lecture 12: Overview

- Top-Down Embedded Design Flow
 - Specification Modeling Guidelines
- System-on-Chip Environment (SCE)
 - Design Example: GSM Vocoder
 - Profiling and performance estimation
 - Interactive demonstration
- Homework Assignment 7
 - Performance estimation of the Canny Edge Detector



Specification Modeling Guidelines

- Example: Guidelines for SoC Environment (SCE)
 - Clean behavioral hierarchy
 - hierarchical behaviors:
no code other than par, pipe, seq, fsm, and try-trap statements
 - leaf behaviors:
Pure ANSI-C code (no SpecC constructs)
 - Clean communication
 - point-to-point communication via standard channels
 - ports of plain type or interface type, no pointers
 - port maps to local variables or ports only
- Detailed rules for SoC Environment
 - CECS Technical Report:
“*SCE Specification Model Reference Manual*”
by A. Gerstlauer, R. Dömer, et al.
 - `/opt/sce-20100908/doc/SpecRM.pdf`

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Specification Modeling Guidelines

- Converting C reference code to SpecC
 - Major functions become behaviors
 - Function call tree becomes behavioral hierarchy
 - Function call becomes behavior instance call
 - Sequential statements become leaf behaviors
 - Control flow becomes FSM
 - Conditional statements: `if`, `if-else`, `switch`
 - Loops: `while`, `for`, `do-while`
 - Explicitly specify potential parallelism
 - Explicitly specify communication
 - Use standard channels, avoid shared variables
 - No global variables
 - Only local variables in behaviors and functions/methods
 - Data types
 - Avoid dynamic memory allocation
 - Avoid pointers (arrays are preferred)
 - Use explicit data types if suitable (e.g. bit vectors)

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System-on-Chip Environment (SCE)

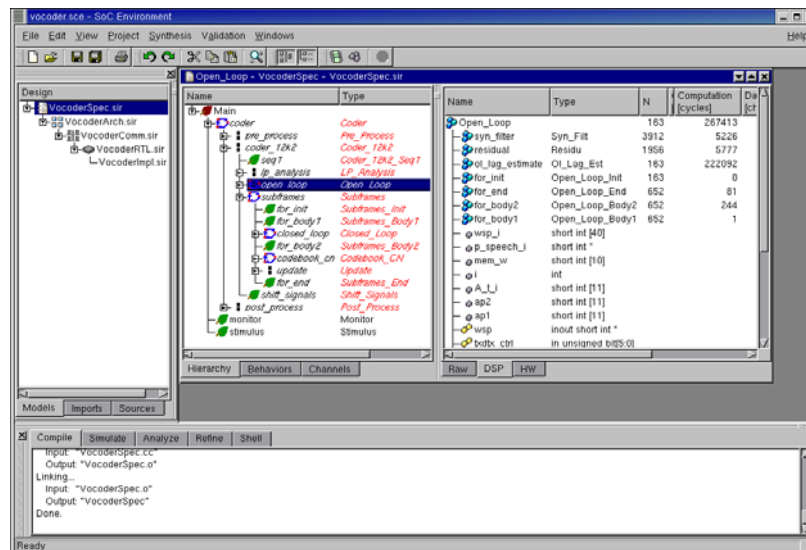
- Integrated Development Environment (IDE) with support of:
 - Graphical frontend (*sce*, *scchart*)
 - SLDL-aware editor (*sced*)
 - Compiler and simulator (*scc*)
 - Profiling and analysis (*scprof*)
 - Architecture refinement (*scar*)
 - RTOS refinement (*scos*)
 - Communication refinement (*sccr*)
 - RTL refinement (*scrtl1*)
 - Software refinement (*sc2c*)
 - Scripting interface (*scsh*)
 - Tools and utilities (*sir_list*, *sir_tree*, ...)

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SCE Main Window



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SCE Source Editor

The screenshot shows the SCE Source Editor interface. On the left, a project tree displays the hierarchy: `VocoderSpec.sir` (Main) containing `VocoderArch.sir`, `VocoderComm.sir`, `VocoderRTL.sir`, and `VocoderImpl.sir`. The `VocoderImpl.sir` sub-tree includes `pre_process`, `coder_12k2`, `seg7`, `subframes`, `for_init`, `for_body`, `for_body2`, `for_end`, `codebook`, `for_end`, `update`, `for_end`, `shift_signals`, `monitor`, and `post_process`. The main editor window shows the following code:

```

behavior Coder_12k2_Seq1(
    in  Word16 speech_proc[L_FRAME],
    Word16 old_speech[L_TOTAL],
    Word16 *speech,
    out  Word16 *p_window,
    Word16 old_wsp[L_FRAME + PIT_MAK],
    out  Word16 *wsp,
    Word16 old_exe[L_FRAME + PIT_MAK + L_INTERPOL],
    out  Word16 *exc,
    out  Flag  patch,
    out  DTCtrl txtx_ctrl,
    in  Flag  reset_flag
)

implements Ireset
{
void init(void)
{
    /* Initialize pointers to speech vector. */

    speech = old_speech + L_TOTAL - L_FRAME; /* New speech */
    p_window = old_speech + L_TOTAL - L_WINDOW; /* For LPC window */

    /* Initialize pointers */

    wsp = old_wsp + PIT_MAK;
    exc = old_exc + PIT_MAK + L_INTERPOL;

    /* vectors to zero */

    Set_zero (old_speech, L_TOTAL);
    Set_zero (old_exc, PIT_MAK + L_INTERPOL);
    Set_zero (old_wsp, PIT_MAK);

    txtx_ctrl = TX_SP_FLAG | TX_VAD_FLAG;
    patch = 1;
}
}
    
```

At the bottom of the window, the status bar indicates 'INS Line: 62 Col: 6'.

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SCE Hierarchy Displays

The screenshot displays two hierarchy charts. The left chart, titled 'Open_Loop - VocoderSpec - SpecC Hierarchy Chart', shows a vertical flow of components: `for_init`, `for_body`, `for_body2` (which contains `weight_at_1` and `weight_at_2`), `residual`, and `spe_filter`. The right chart, titled 'Coder - VocoderComm - SpecC Hierarchy Chart', shows a more complex structure with `for_DSP` and `for_DSP` blocks at the top, connected to `book_CH_M` and `book_CH_M` blocks, which then connect to `DSP` and `HW` blocks at the bottom.

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SCE Compiler and Simulator

The screenshot shows the SCE Environment interface. The main window displays the following text:

```

European digital cellular telecommunications system
12200 bit/s speech code for
enhanced full rate speech traffic channels

Bit-Exact Spec: Simulation Code - encoder
Version 1.0
March 15, 1999

BITx: disabled
Input speech file: speechfiles/spch_uns.inp
Output bitstream file: routx.bit

Frames 1 encoding delay = 0,00 ms
Frames 2 encoding delay = 0,00 ms
Frames 3 encoding delay = 0,00 ms
Frames 4 encoding delay = 0,00 ms
Frames 5 encoding delay = 0,00 ms
Frames 6 encoding delay = 0,00 ms
Frames 7 encoding delay = 0,00 ms
Frames 8 encoding delay = 0,00 ms
Frames 9 encoding delay = 0,00 ms
Frames 10 encoding delay = 0,00 ms
Frames 11 encoding delay = 0,00 ms
Frames 12 encoding delay = 0,00 ms
Frames 13 encoding delay = 0,00 ms
Frames 14 encoding delay = 0,00 ms
Frames 15 encoding delay = 0,00 ms
Frames 16 encoding delay = 0,00 ms
Frames 17 encoding delay = 0,00 ms
Frames 18 encoding delay = 0,00 ms
Frames 19 encoding delay = 0,00 ms
Frames 20 encoding delay = 0,00 ms
Frames 21 encoding delay = 0,00 ms
Frames 22 encoding delay = 0,00 ms
Frames 23 encoding delay = 0,00 ms
Frames 24 encoding delay = 0,00 ms
Frames 25 encoding delay = 0,00 ms
Frames 26 encoding delay = 0,00 ms
Frames 27 encoding delay = 0,00 ms
    
```

Below the main window, the console shows the compilation process:

```

scc: SpecC Compiler V 2.2 a
(c) 1997-2000 CECS, University of California, Irvine

Importing...
Input: "VocoderSpec.ins.sir"
Output: <internal representation>
Translating...
Input: <internal representation>
Output: "VocoderSpec.h"
Output: "VocoderSpec.cc"
Compiling...
Input: "VocoderSpec.cc"
Output: "VocoderSpec.o"
Linking...
Input: "VocoderSpec.o"
Output: "VocoderSpec"
Done.
    
```

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SCE Profiling and Analysis

The screenshot displays the SCE Profiling and Analysis interface. The main window shows an "Operation Profile" bar chart with the following data:

Category	Rel. seconds
codebook_cn	~8.0
closed_loop	~6.5
open_loop	~4.5
lp_analysis	~4.5

Below the chart is a table of code statistics:

Type	N	Computation [cycles]
codebook_cn	652	8617
Q_Gain_Code	652	1250
Ex_Syn_Upd_Sh	652	7367

Three pie charts provide detailed analysis of the codebook_cn component:

- codebook_cn - Operation Chart:** Shows the distribution of operations within the codebook_cn component.
- Int ALU:** Shows the distribution of operations within the integer ALU component.
- Int Arith:** Shows the distribution of operations within the integer arithmetic component.

The console window at the bottom shows the profiling process:

```

generating internal data structure for profiling
Deriving raw statistics from SIR file
Computing weighted statistics
Annotating weighted statistics to SIR file
End: retargetable profiling
    
```

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SCE Demonstration

- Application Example: GSM Vocoder
 - Enhanced full-rate voice codec
 - GSM standard for mobile telephony (GSM 06.10)
 - Lossy voice encoding/decoding
 - Incoming speech samples @ 104 kbit/s
 - Encoded bit stream @ 12.2 kbit/s
 - Frames of $4 \times 40 = 160$ samples ($4 \times 5\text{ms} = 20\text{ms}$ of speech)
 - Real-time constraint:
 - max. 20ms per speech frame
(max. total of 3.26s for sample speech file)
 - SpecC specification model
 - 29 hierarchical behaviors (9 par, 10 seq, 10 fsm)
 - 73 leaf behaviors
 - 9139 formatted lines of SpecC code
(~13000 lines of original C code, including comments)

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SCE Demonstration

- Application Example: GSM Vocoder
 - Exploration of Specification Model
 - Simulation
 - Profiling
 - Performance estimation
 - Interactive demonstration

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Project Assignment 7

- Task: Performance Estimation of the Canny Example
 - Profiling to estimate relative computational complexity
 - Instrumentation to measure absolute timing as reference
- Steps
 1. Profile the application, identify performance bottlenecks
 - Relative complexity: Use GNU profiling tools
 2. Instrument the application, measure timing on reference platform
 - Absolute timing: Use Linux timing APIs
- Deliverable
 - `canny.txt` (including tables of obtained results)
- Due
 - February 19, 2020, 6pm (combined with A6)

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Project Assignment 7

- Performance Estimation of the Canny Edge Detector
- Step 1: Profile the application components , obtain relative computational complexity
 - Use a provided C++ model (derived from SpecC model)
 - Use GNU profiling tools
 - `g++ -pg, gprof`
 - Compile the SystemC source code with option `-pg`
 - Run the simulation once (with instrumentation, `gmon.out`)
 - Run the profiler: `gprof Canny`
 - Validate the reported call tree
 - Analyze the “flat profile” for the DUT components
 - Select the main functions of interest

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Project Assignment 7

- Step 1: Profile the application components, obtain relative computational complexity
 - Expected complexity comparison (in `canny.txt`):

```

Gaussian_Smooth          ...%
|----- Receive_Image   ...%
|----- Gaussian_Kernel ...%
|----- BlurX           ...%
\----- BlurY           ...%
Derivative_X_Y           ...%
Magnitude_X_Y            ...%
Non_Max_Supp             ...%
Apply_Hysteresis         ...%
                        100%

```

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Project Assignment 7

- Step 2: Instrument the application components, obtain absolute timing on reference platform
 - Since we do not have a prototyping platform available, we use the department server as reference
 - Instrument your model source code:

```

#include <time.h>
clock_t Tstart, Tstop;
double T1 = 0.0;
...
Tstart = clock();
f();
Tstop = clock();
T1 = (double)(Tstop-Tstart)/CLOCKS_PER_SEC;

```

- Use global variables for this temporary instrumentation

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Project Assignment 7

- Step 2: Instrument the application components, obtain absolute timing on reference platform
 - Expected complexity comparison (also in `canny.txt`):

```

Gaussian_Smooth                ...sec ...%
|----- Receive_Image         ...sec ...%
|----- Gaussian_Kernel       ...sec ...%
|----- BlurX                  ...sec ...%
\----- BlurY                  ...sec ...%
Derivative_X_Y                  ...sec ...%
Magnitude_X_Y                   ...sec ...%
Non_Max_Supp                    ...sec ...%
Apply_Hysteresis                ...sec ...%
                                100%

```