Interconnect Energy Dissipation in High-Speed ULSI Circuits

PayamHeydari
Department of Electrical Engineering and Computer Science
University of California
Irvine, CA 92697

Soroush Abbaspour and Massoud Pedram
Department of Electrical Engineering-Systems
University of Southern California
Los Angeles, CA 90089

Abstract - *This paper presents a detailed empirical study and analytical derivation of voltage waveform and energy dissipation of global lines driven by CMOS drivers. It is shown that at high clock frequencies where the output voltage at the termination point of the transmission line may not reach its steady state value during the clock period, it is possible to reduce energy dissipation while meeting a DC noise margin by driver sizing. This is in sharp contrast with the steady state analysis, which states that driver size has no impact on the energy dissipation per output change. In addition, we propose a new design metric which is the product of energy, delay and some measure of ringing in lossy transmission lines. In particular, this paper provides closed-form expressions for the energy dissipation, 50% propagation delay and the percentage of maximum undershoot when the circuit exhibits an underdamped behavior. This metric is used during the driver sizing problem formulation for minimum energy-delay-ringing product. The experimental results carried out by HSPICE simulation verify the accuracy of our models.*

1. INTRODUCTION

New Advances in CMOS technologies has tremendously improved the integration capability and the speed of operation and reduced the amount of energy consumed per signal transition. Technology scaling with 30% reduction in minimum feature size per generation results in: (1) gate delay reduction by 30%, (2) doubling of the number of transistors that fit in the same silicon area (3) energy reduction per transition by 30% to 65% depending on the degree of accompanying supply voltage scaling. These technology-induced

improvements, coupled with advances in circuits and microarchitecture design, are expected to continue to support and to sustain the Moore's law until year 2014 [1].

The wiring system of a one-billion transistor die will deliver signal and power to each transistor on the chip, provide low-skew and low-jitter clock to latches, flip-flops and dynamic circuits, and also distribute data and control signals throughout the chip [2]. Providing the required global connectivity throughout the whole chip demands long on-chip wires. These global wires should deliver high frequency signals (presently at around 1-2GHz) to various circuits. This implies that the global wires exhibit transmission line effects including electromagnetic coupling. On the other hand, as technology sizes continue to decrease, many new effects are being observed due to the use of nanometer technologies. Some significant deep sub-quarter-micron effects are caused by increasing cross-coupling capacitance and coupling inductance. So far, the well-known $(1/2)CV^2$ model has been used as an interconnect energy model, where C includes the capacitance of the interconnect as well as the capacitances of driving and driven circuitries, and V is the voltage swing. This model, however, fails to predict the interconnect energy dissipation in the current range of clock frequencies, where the signal transients do not settle to a steady state value due to the small clock cycle-time. Moreover, this model does not consider coupling noise being imposed by neighboring wires as well as other transmission line properties. As we will see in this paper, these effects must be taken into account in the energy calculations, that will otherwise lead to erroneous results. An analytical interconnect energy model with consideration of event coupling has been proposed in [3]. The authors used nodal equations for a system of interconnects to obtain the state vector of the system. The state vectors were utilized in the interconnect energy dissipation expression. This approach does not capture the transmission line effects. It also assumes that the system reaches the steady-state. In [4], authors showed that using distributed RC circuits do not capture all behaviors of lossy transmission lines that can be captured otherwise using the transmission line equations. Taylor *et al.* proposed a deep sub-micron (DSM) aware power estimation methodology using a three-wire lookup table [5]. The dissipated energy of each individual interconnect is computed considering capacitive coupling effects of the immediate adjacent wires. Using a detailed SPICE simulation of all possible types of transitions on a group of three adjacent wires, a three-wire lookup table was created. To obtain the total energy dissipation, the sum of energy dissipations of each individual interconnect was computed [5]. Reference [5], however, does not consider the transient behavior of the interconnect in the energy calculations.

In this paper, accurate expressions for the energy dissipation of coupled interconnects are obtained while addressing the transmission line effects on the energy dissipations. We provide empirical evidence as well as detailed closed-form analytical expressions for the energy dissipation of a lossy transmission line which is driven by a CMOS inverter and is terminated by a CMOS load. We show that this circuit configuration

exhibits behavior similar to a new RLC circuit topology, and therefore, it is possible to reduce energy dissipation at a given clock frequency by driver sizing. The effect of driver sizing is to change the output behavior (from over-damped to under-damped or vice versa). By careful selection of W/L ratio of the line driver, we may thus reduce the overall energy dissipation of the line and line driver. This is accomplished by forcing the input transition to initiate when the output is in the undershoot region (for the underdamped case), or by forcing the input transition to take place when the output has met the DC noise margin, but not yet reached the steady state (for overdamped case). Clearly, there are some critical design metrics that need to be taken into consideration during the driver sizing, such as propagation delay and the ringing. We, therefore, present a driver sizing technique that minimizes energy-delay-ringing product.

Section 2 presents two circuit model for the lossy transmission line; an RLC circuit configuration called RLC-π circuit, and an RLC circuit. In section 3, the RLC-π and the RLC circuits are utilized to derive the total energy dissipation of a transmission line driven by a CMOS inverter for large W/L's and small W/L's of the driving transistors, respectively. Then a new metric is utilized that is very relevant for the energy optimization under the delay constraint. Simulations and experimental results provided throughout this section confirms the accuracy of our model and the usefulness of our metric. Finally, section 4 presents the conclusions of our paper.

2. ENERGY DISSIPATION OF PASSIVE RLC CIRCUITS

A common way of studying the parasitic effects of an on-chip interconnect on the performance of a VLSI circuit is to model it using a large number of cascaded ladder RLC circuits. Therefore, a relevant starting point to study the energy dissipation of on-chip interconnects is to investigate the energy dissipation of a passive RLC circuit, depicted in Fig. 1, that is excited by a unit-step voltage. Depending on the relative values of the circuit elements, this circuit exhibits one of the two possible transient responses as also depicted in Fig. 1.

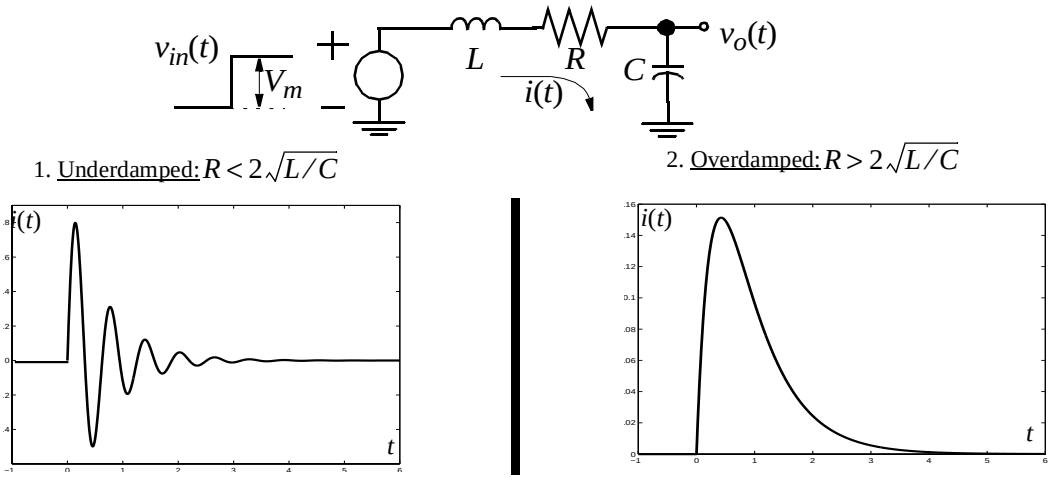


Fig. 1. An RLC circuit excited by a unit-step voltage. Current waveforms are shown for both the underdamped and the overdamped cases.

The total energy delivered by the input source to the passive circuit is as follows:

$$E_{tot} = \int_{-\infty}^{\infty} v_{in}(t) i(t) dt \tag{1}$$

In the next two sub-sections, we obtain the total as well as the dissipated energy for both underdamped and overdamped RLC circuits.

2.1. Energy dissipation of an underdamped RLC circuit

In the underdamped case, the voltage and current transient waveforms oscillate toward their steady-state values. This transient behavior occurs when $R < 2\sqrt{L/C}$. In terms of energy, the stored energy in the capacitor and/or in the inductor is being transferred back and forth between reactive elements. If the circuit is lossless (R = 0), this energy transfer will be performed endlessly. However, with a resistor being present in the circuit, a portion of the energy is dissipated in the resistor. To obtain the energy dissipated by the circuit, we first obtain the total energy generated by the input source.

$$E_{u,\,tot} = \int_{0}^{\infty} V_m i_u(t) dt \tag{2}$$

where $i_u(t)$ is the current flowing through the underdamped circuit [in Fig. 1, $i(t) = i_u(t)$].

Suppose that the input source to the RLC circuit is a periodic rectangular waveform, which is almost the case in digital integrated circuits. The total energy delivered by the input source during a low-to-high transition of the input source is as follows:

$$E_{u,\,tot}^{RLC} = CV_m^2\left[1-\left(\frac{\omega_{n_0}}{\omega_{d_0}}\right)e^{-\frac{\alpha_0 T}{2}}\sin\left(\frac{\omega_{d_0}T}{2}+\Phi_0\right)\right] \tag{3}$$

where α_0, the damping constant, is $\alpha_0 = R/2L$, ω_{n0}, the resonant frequency, is $\omega_{n_0} = 1/\sqrt{LC}$, and ω_{d0}, the oscillation frequency, is equal to $\omega_{d_0} = \sqrt{\omega_{n_0}^2 - \alpha_0^2}$.

Fig. 2 shows the energy variation as a function of the fundamental period, *T*, for an underdamped RLC circuit excited by a periodic rectangular voltage signal. Note that for small periods, the $(1/2)CV^2$ energy model gives rise to a wrong value.

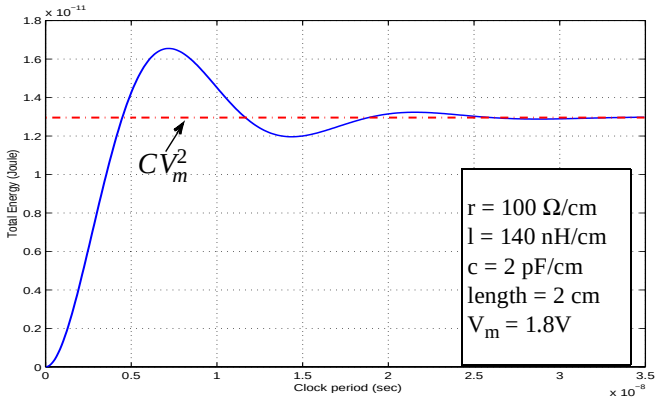


Fig. 2. The total delivered energy vs. the fundamental periods of oscillations for an underdamped RLC circuit

The dissipated energy in the low-to-high transition of the input source is:

$$E_{u,\,dissipated}^{L\to H} = \int_0^{T/2} Ri_u^2(t)dt = \frac{1}{2}CV_m^2\left[1-\left(\frac{\omega_{n_0}}{\omega_{d_0}}\right)^2 e^{-\alpha_0 T}(1-\cos(\omega_{d_0}T-\Phi_0)\cos(\Phi_0)\right] \tag{4}$$

In equations (3) and (4), $\Phi_0 = \text{atan}(\omega_{d_0}/\alpha_0)$. As *T* increases, the second term inside the bracket becomes smaller, and in the limit, the energy expression simply becomes $(1/2)CV_m^2$.

❐

2.2. Energy dissipation of an overdamped RLC circuit

In the overdamped case, the resistor is sufficiently large (i.e., $R > 2\sqrt{L/C}$) to eliminate resonances from current and voltage waveforms. The total energy delivered by the input source is the same as Eq. (1), which is rewritten here for convenience.

$$E_{o,\,tot} = \int_0^{\infty} V_m i_o(t)dt \tag{5}$$

where $i_o(t)$ is the current flowing through the overdamped circuit [in Fig. 1, $i(t) = i_o(t)$]. Similar to the underdamped case, consider a periodic rectangular waveform at the input. The total energy delivered by the input source is:

$$E_{o,\,tot}^{RLC} = V_m^2\left[1-\left(\frac{\omega_{n_0}}{\alpha_{d_0}}\right)e^{-\frac{\alpha_0 T}{2}}\sinh\left(\frac{\alpha_{d_0}T}{2}+\Psi_0\right)\right] \tag{6}$$

Fig. 3 shows the energy variation in terms of the variation in the fundamental period. The error caused by using the $(1/2)CV^2$ model in the overdamped case is smaller than that in the underdamped case. However, in practice, the underdamped response occurs more frequently in practical situations, because the on-chip interconnect resistive loss is small, particularly for circuits fabricated in copper technology.

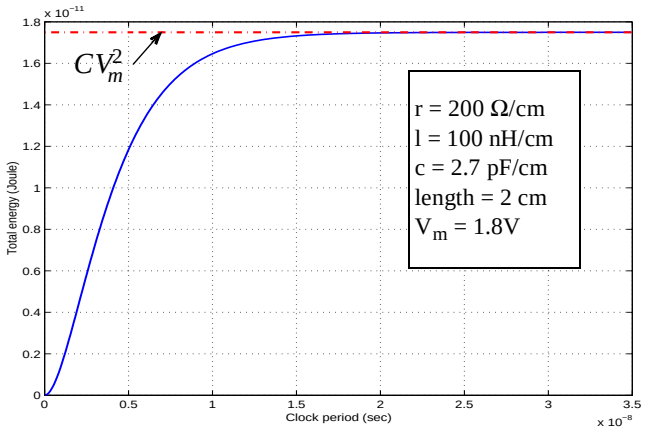


Fig. 3. The total delivered energy vs. the fundamental periods of oscillations for an overdamped RLC circuit

The energy dissipated in the low-to-high transition of the input source will be as follows:

$$E_{o,\,dissipated}^{L\to H} = \frac{1}{2}CV_m^2\left[1+\left(\frac{\omega_{n_0}}{\alpha_{d_0}}\right)^2 e^{-\alpha_0 T}\left(1-\cosh(\alpha_{d_0}T+\Psi_0)\cosh(\Psi_0)\right)\right] \tag{7}$$

In equations (6) and (7), $\Psi_0 = \operatorname{atanh}(\alpha_{d_0}/\alpha_0)$. Once again, as T increases, the energy expression approaches $(1/2)CV_m^2$.

❐

2.3. Frequency-domain analysis

Some observations can be made from the foregoing analysis. First of all, the energy dissipation of a passive RLC circuit excited by a *unit-step* input of amplitude V_m is $(1/2)CV_m^2$ irrespective of the circuit response (i.e., overdamped or underdamped). From another perspective, the capacitor charges up to the input step

voltage, V_m, and in the steady-state is modeled as an open circuit. Therefore, the total stored energy appears as electric field energy across the capacitor ($(1/2)CV_m^2$).

An important task is to find a simple equivalent circuit corresponding to a given RLC circuit that can be directly utilized to obtain the total energy generated by the input source. To find such equivalent circuit, first consider the driving-point admittance of RLC circuit of Fig. 1.

$$Y_{in}(s) = \frac{s/L}{s^2 + 2\alpha_0 s + \omega_{n_0}^2} \tag{8}$$

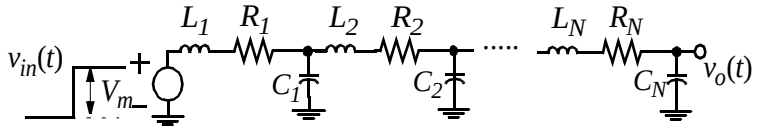
$Y_{in}(s \to 0)$ represents the equivalent DC driving-point admittance of the circuit in the steady-state. This simple observation will be used later during the simplification of the driving-point admittance as well as the derivation of the energy dissipation of a coupled lossy transmission line. Simple calculation reveal that for the RLC circuit shown in Fig. 1, $Y_{in}(s \to 0) = Cs$. The current flowing to the circuit is thus an impulse function, and the total delivered energy by the source is as follows:

$$E_{tot} = \int_0^\infty V_m i(t)dt = \int_0^\infty V_m^2 C\delta(t)dt = CV_m^2 \tag{9}$$

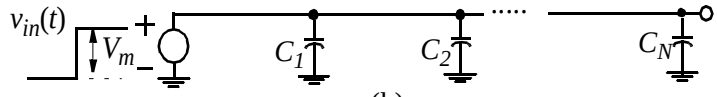
As a consequence, the energy transferred from the unit-step voltage source to the RLC circuit of Fig. 1 is the same as the energy delivered by the unit-step source to the low-frequency component of the driving-point admittance of this RLC circuit. For the RLC circuit in Fig. 1, this low-frequency component is the capacitor.

As a generalization, consider a circuit consisting of N RLC circuits in cascade that is excited with a unit-step voltage, as shown in Fig. 4 (a). The equivalent circuit for each RLC subsection solely consists of the capacitor of the RLC subsection. As a consequence, the equivalent circuit for the circuit of Fig. 4 (a) is an all-capacitive circuit shown in Fig. 4 (b). The total energy delivered by the source in the steady-state is:

$$E_{tot} = \int_0^\infty V_m i(t)dt = \left(\sum_{k=1}^{N} C_k \right) V_m^2 \tag{10}$$



(a)



(b)

Fig. 4. A ladder of cascaded RLC circuits. (a) the circuit schematic, (b) the equivalent circuit for the energy analysis.

Eq. (10) is in agreement with the well-known CV^2 model for the on-chip interconnect. Although Eq. (10) reiterates a well-known concept, the discussion that was undertaken to derive (15) will, however, play a key role in our analysis of the interconnect energy dissipation.

3. ENERGY DISSIPATION OF LOSSY TRANSMISSION LINES

So far, our main attention has focused on the energy analysis of single passive RLC circuits. There are, however, two major questions that also need to be addressed. In present-day digital and mixed-signal integrated circuits, the global on-chip interconnects must provide the required connectivity and performance for clock rates of 1.0-3.0GHz, which is in a microwave frequency range. This certainly demands a knowledge of electromagnetic-field theory to analyze the on-chip wiring effects. A related question that arises is whether the transmission line effects of on-chip interconnects can have any effect on the energy dissipation. On the other hand, high wiring density and high operating frequencies result in high capacitive and inductive coupling. Consequently, the second question is whether the electromagnetic coupling has any impact on the energy dissipation. This section addresses these questions.

The critical global interconnections, such as clock lines, control lines, and data buses (which can be 32-128 bits wide) between processor and on-chip cache reach more than 100K connections [2]. The propagation delay of signals traveling through these global wires is comparable to the time of flight. In other words, the line length is comparable to the propagated signal wavelength, λ, which is on the order of 0.7-2.2cm. This implies that transmission-line properties have to be taken into account. It was shown in [4] that any two uniform parallel conductors, the signal and the return paths, that are used to transmit electromagnetic energy can be considered transmission lines. The return path can be a ground plane, a ground conductor, or a mesh of ground lines on many layers. Solutions to Maxwell's equations for the electric and magnetic fields around conductors are current and voltage waves. The current and voltage wave solutions are a function of the characteristic impedance, Z_o, and the propagation constant, γ. Consider a single transmission line as shown in Fig. 5. Note that the on-chip long wires are implemented in the top-level metal layer (for instance, metal 6 in 0.18μm technology). The top-level metal layers are far above the substrate and isolated from lower-level metal layers using interlayer dielectric material. Therefore, the shunt resistance is very large, and hence is orders of magnitudes larger than the capacitance reactance at current clock frequencies. Therefore, the per-unit shunt conductance is ignored in the circuit representation of Fig. 5.

The voltage and current waves in the frequency domain at any point *x* along the line are expressed as a combination of incident and reflected waves.

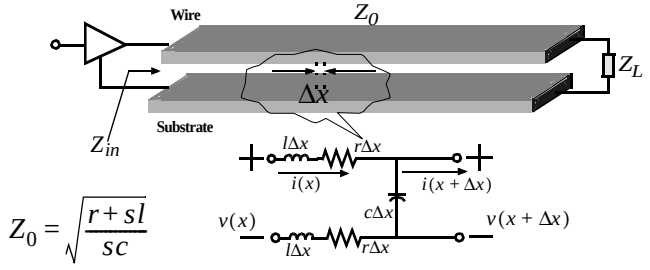


Fig. 5. The schematic of a lossy transmission line along with the circuit representation of a differential length Δx

$$V(x,s) = V_i e^{-\gamma x} + V_r e^{\gamma x} \tag{11}$$

$$I(x,s) = I_i e^{-\gamma x} - I_r e^{\gamma x} \tag{12}$$

where $\gamma = \sqrt{(r+sl)cs}$. The load termination determines how much of the wave is reflected upon arrival at the wire end. The *reflection coefficient*, Γ_L , determines the amount of the incident wave that is reflected back to the line as a result of impedance mismatch between the line and the load.

$$\Gamma_L = \frac{Z_L - Z_0}{Z_L + Z_0} \tag{13}$$

The concept of the reflection coefficient is generalized to define the reflected and incident quantities at any arbitrary point along the line.

$$\Gamma(x) = \frac{V_r(0)e^{\gamma x}}{V_i(0)e^{-\gamma x}} = \Gamma_L e^{2\gamma x} \tag{14}$$

The driving point impedance, Z_{in}, of the lossy line terminated by a load impedance Z_L is the ratio of the voltage and current waves at the input source end.

$$Z_{in}\big|_{x=-h} = \frac{V_i e^{\gamma h} + V_r e^{-\gamma h}}{I_i e^{\gamma h} - I_r e^{-\gamma h}} = Z_0\left(\frac{1+\Gamma_L e^{-2\gamma h}}{1-\Gamma_L e^{-2\gamma h}}\right) = Z_0 \frac{Z_L + Z_0 \tanh(\gamma h)}{Z_0 + Z_L \tanh(\gamma h)} \tag{15}$$

where *h* is the line length. In the above equation, the load impedance, Z_L, is normally the input capacitance of driven CMOS circuits following the line.

To account for the electromagnetic coupling effects in the interconnect energy dissipation, the total line inductance and capacitance per unit length are modified accordingly. The effect of capacitive coupling is predicted by considering the switching transients of the immediate neighboring wires. The effect of nonadjacent lines are ignored because the capacitive coupling exhibits a near-field effect, and the adjacent

aggressive lines behave as shield lines for non-adjacent wires. On the contrary, the inductive coupling exhibits a far-field effect. The non-adjacent lines have a considerable amount of inductive couplings on the victim line. This makes the analysis of inductive coupling particularly difficult. In addition, the current return paths cannot be easily configured in the circuit [4]. This causes the problem of inductive coupling to become even more complicated.

The effect of capacitive coupling is taken into account by using an alternative adaptation of the Miller theorem [6] for traveling wave equations, as also shown in Fig. 6. The Miller capacitance per unit length seen across the input port of the transmission line 1 as a result of switching in line 2 is:

$$c_{c,M} = c_c\left(1 - \frac{V_2(-h, s)}{V_1(-h, s)}\right) \tag{16}$$

The voltage waves V_2 and V_1 are obtained by combining their incident and reflected wave components at their corresponding output terminal ports. To verify the accuracy of Eq. (16), a circuit consisting of two neighboring micro-strip lines, each of which terminated by a 200fF capacitor, and excited by a voltage square-wave is simulated with HSPICE. The input voltages to these two adjacent lines are in opposite phase. The geometrical description of lines is denoted in Fig. 6.

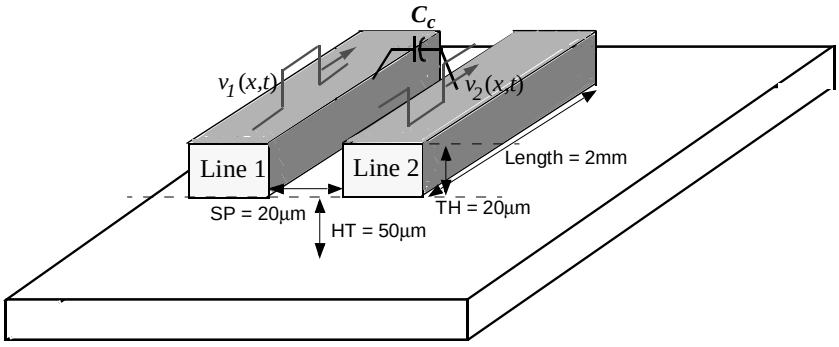


Fig. 6. Two capacitively coupled transmission lines. The traveling voltage waves are 180◦ out of phase.

Fig. 7 (a) shows current and voltage waveforms of line 1. Line 1 is then decoupled from line 2 by replacing cross-coupling capacitance c_c with its Miller capacitance $c_{c,M}$ from line 1 to ground-plane, and then simulate this new circuit with HSPICE again. The voltage and current waveforms are depicted in Fig. 7 (b). Comparing voltage and current waveforms in Fig. 7 (a) with those in Fig. 7 (b) verifies the accuracy of Eq. (16).

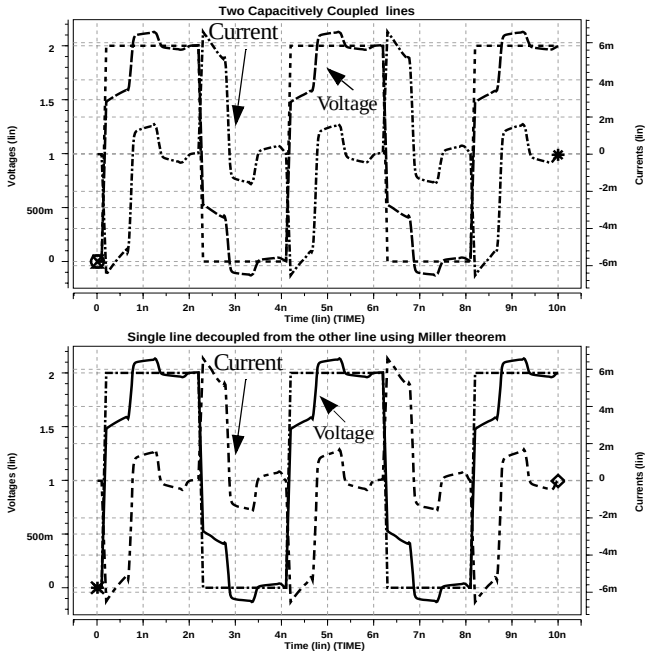


Fig. 7. The source voltage as well as driving-point current and voltage waveforms in a lossy coupled transmission line. (a) results obtained using HSPICE simulation on the coupled line. (b) results obtained using HSPICE on the decoupled line after applying Miller theorem

The inductive coupling between the lines is far more complicated phenomenon than the capacitive coupling. First of all, unlike the capacitive coupling, it presents a far-field effect, therefore, the inductive coupling of non-adjacent lines must be accounted for. To simplify the analysis, the inductive coupling is addressed for the bus structures in which constituting parallel lines have identical geometries and carry the same currents. For example, in a set of N coupled bus lines, the total per unit length inductance of the j-th line that is magnetically coupled to other lines is:

$$l_{int,tot_j} = l_{int_j} + \sum_{i \neq j} (\pm M_{ij}) \tag{17}$$

Note that if the currents are not equal, we cannot reduce an n-port coupling to a single scalar form, i.e., the coupling should be expressed in a matrix form.

❒

According to Eq. (15), the input impedance of a transmission line is a nonlinear function of frequency. Unfortunately, direct substitution of this nonlinear expression into the energy equation (which is the integral of the voltage-current product) does not yield a closed-form expression for the energy dissipation of

the lossy transmission line. Yet, it is possible to simplify Eq. (15), using similar observations in Section 2.3, and obtain an accurate expression for the energy dissipation.

Observation 1. If the transitions of the input waveform to a circuit are sufficiently spaced apart so as to allow the circuit to come very close to its steady-state response, then the total energy delivered by the input source is obtained using the driving-point impedance of the circuit evaluated at low frequencies.

This observation is utilized here to simplify Eq. (15). We evaluate *tanh*(.) at low frequencies by expanding its Taylor expansion around $s = 0$ and truncating higher order terms. Depending upon the order of the truncation, two stable equivalent circuits are extracted.

To account for the interconnect propagation delay, the signal transfer function from the input of the line driver to the output terminal of the interconnect must also be calculated. Therefore, in addition to developing an equivalent circuit for the driving-point impedance, an equivalent circuit must also be constructed for the signal transfer function. This will be discussed in Section 3.2.

A. First-order truncation

The first-order Taylor expansion of $\tanh(\gamma h)$ is γh. This leads to the following approximated rational function:

$$Z_{in}\Big|_{x=-h} = \frac{1}{C_L s}\left[\frac{1+\left(\gamma^2 h^2 \dfrac{C_L}{C_{int,tot}}\right)}{1+\dfrac{C_{int,tot}}{C_L}}\right] \tag{18}$$

where $C_{int,tot}$ is the total interconnect capacitance including the Miller capacitance of the neighboring lines that are capacitively coupled to the line, and the interconnect-to-substrate capacitance. Using Eq. (18) a series RLC circuit is synthesized as depicted in Fig. 8, where R_{eq} and L_{eq} are defined as follows:

$$R_{eq} = \frac{C_L}{C_L + C_{int,tot}} R_{int} \quad , \quad L_{eq} = \frac{C_L}{C_L + C_{int,tot}} L_{int,tot} \tag{19}$$

R_{int} is the line resistance. $L_{int,tot}$ is the total inductance of the lossy line including the self and mutual inductances and is obtained by Eq. (18). The inductive couplings between transmission lines are accounted for by an algebraic summation of each line's self inductance and all mutual inductances between that line and other lines considering also the current direction flowing through the lines.

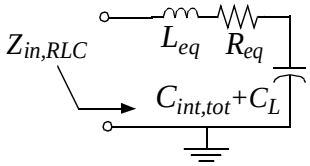


Fig. 8. The circuit realization of Eq. (19)

B. Second-order truncation

The second-order truncation of the Taylor series expansion of *tanh*(γ*h*) is:

$$\tanh(\gamma h) = \frac{\sinh(\gamma h)}{\cosh(\gamma h)} \rightarrow \frac{2\gamma h}{2+\gamma^2 h^2} \quad , \textit{ for small values of } |s| \quad (20)$$

Recall that γ is a function of *s*. Replacing *tanh*(γ*h*) in Eq. (15) with its second-order truncation leads to the following relationship:

$$Z_{in}\big|_{x=-h} = \frac{1}{C_L s}\left[\frac{2+\gamma^2 h^2 + \left(2\gamma^2 h^2 \frac{C_L}{C_{int,tot}}\right)}{2+\gamma^2 h^2 + \left(2\frac{C_{int,tot}}{C_L}\right)}\right] \quad (21)$$

To find out the accuracy of Eq. (21) in predicting the frequency variations of the actual driving-point impedance of a lossy line, the driving-point impedance of a single lossy microstrip line driving a 100fF capacitor is calculated using both (15) and (21). The impedance calculations are carried out for three different wire-lengths (length = 0.5mm, 2mm, 9mm). Fig. 9 demonstrates the comparison between the second-order approximation given by (21), and the actual impedance given by (15). On-chip global interconnects with a length of more than 1-2mm are normally broken into smaller segments, and line buffers are inserted between these line segments. For the wire-length of 0.5mm, Eq. (21) accurately follows the frequency variation of the actual input impedance given by Eq. (15) over the whole frequency range of Fig. 9. For the wire-length of 2mm, the truncated second-order impedance successfully follows the variation of the actual impedance of the line for frequencies up to 12GHz.

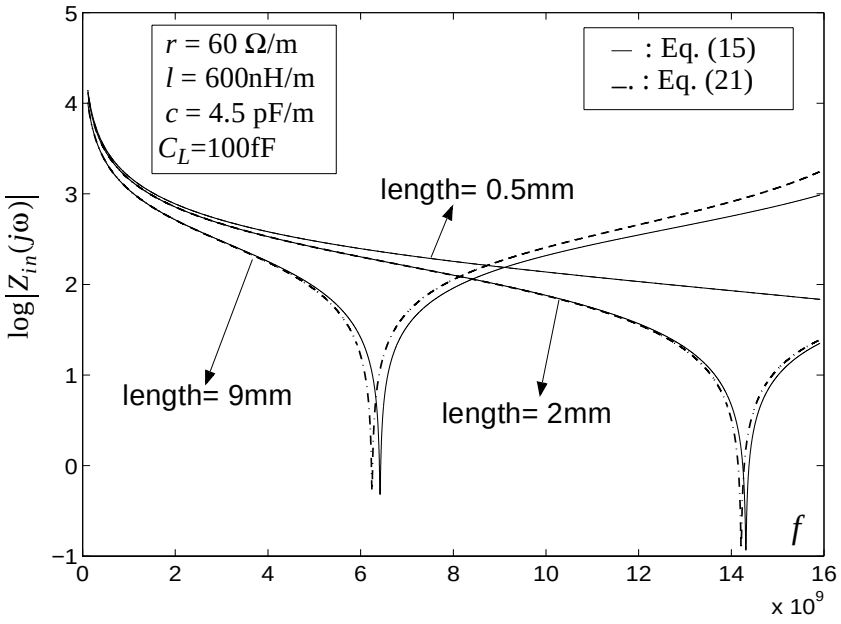


Fig. 9. A comparison between the magnitude response of line's actual driving-point impedance (Eq. (15)) and that of line's approximated rational impedance function (Eq. (21)) for three different line lengths

For the second-order rational function given in (21), a circuit can readily be synthesized. More specifically, for a lossy transmission line whose driving-point impedance near the DC frequency is expressed by Eq. (21), a stable equivalent circuit realization called RLC-π is synthesized whose topology is demonstrated in Fig. 10. The input impedance of the RLC-π circuit shown in Fig. 10 is:

$$Z_{in,\,RLC-\pi}(s) = \frac{1}{(C_1^E + C_2^E \circledS C_3^E)s}\left(\frac{s^2 + \frac{R_{int}}{L_{int,tot}}s + \frac{1}{L_{int,tot}(C_2^E + C_3^E)}}{s^2 + \frac{R_{int}}{L_{int,tot}}s + \frac{(C_1^E + C_3^E)/(C_2 + C_3^E)}{L_{int,tot}(C_1^E + C_2^E \circledS C_3^E)}}\right) \tag{22}$$

where $C_2^E \circledS C_3^E$ represents the series combination of C_2^E and C_3^E. The input impedance of the coupled lossy transmission line in Fig. 10 at the lower-frequency range is:

$$Z_{in,xline}(s) = \left(\frac{1 + 2C_L/C_{int,tot}}{C_L s}\right)\left(\frac{s^2 + \frac{R_{int}}{L_{int,tot}}s + \frac{2}{L_{int,tot}C_{int,tot}(1 + 2C_L/C_{int,tot})}}{s^2 + \frac{R_{int}}{L_{int,tot}}s + \frac{2(1 + C_{int,tot}/C_L)}{L_{int,tot}C_{int,tot}}}\right) \tag{23}$$

Equating $Z_{in,xline}(s)$ with the impedance $Z_{in,\,RLC-\pi}(s)$ of the proposed RLC-π circuit gives values for capacitances C_1^E, C_2^E, and C_3^E:

$$C_3^E = \sqrt{\frac{(C_{int,tot} + C_L)^2 + C_L^2}{2}},\quad C_2^E = \frac{C_{int,tot}}{2} + C_L - C_3^E \qquad C_1^E = C_{int,tot} + C_L - C_3^E \tag{24}$$

Note that C_2^E does not introduce any transmission-zero to the transfer function, because C_1^E-C_2^E-C_3^E make a capacitive loop. This observation is also evident from Eq. (22).

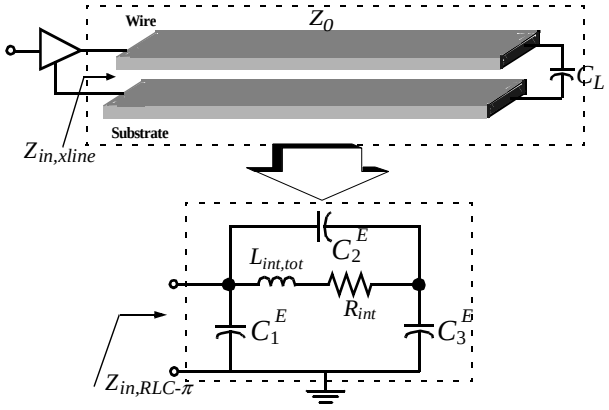


Fig. 10. A lossy transmission line and its equivalent RLC-π circuit representation

Fig. 11 shows the magnitude response of the driving-point admittance of a lossy transmission line which is electromagnetically coupled to a similar line. The line electrical parameters are also indicated in Fig. 11. First, the circuit is simulated using star-HSPICE. In the next step, the magnitude response of the driving-point admittance of the equivalent RLC-π circuit is calculated. According to Fig. 11, this circuit accurately follows the frequency variation of the magnitude response of the line admittance at lower frequencies up to 32GHz. Therefore, according to Observation 1, the energy calculation of the lossy transmission line using the RLC-π circuit yield accurate results. Finally the magnitude response of the driving-point admittance of the equivalent RLC circuit is calculated and compared with those of RLC-π equivalent circuit and the lossy coupled line, as also shown in Fig. 11. The RLC-π circuit models the lossy line more accurately than the RLC circuit over a broader range of frequencies. The discrepancy between the RLC-π circuit and the lossy line at higher frequencies occurs due to the fact that the RLC-π circuit is incapable of modeling the wave reflection phenomenon in a distributed lossy transmission line.

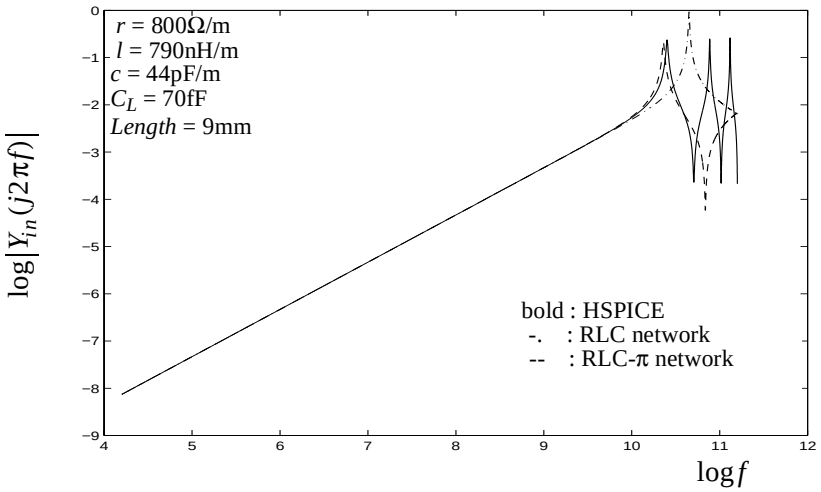


Fig. 11. The magnitude response of the driving-point admittance of an electromagnetically coupled lossy transmission line obtained using HSPICE simulation, and by replacing the line with its equivalent RLC-π circuit, and with its equivalent RLC circuit

The RLC-π circuit is also used to calculate propagation delay of the interconnect, as will be illustrated in Section 4.2. Using the RLC-π circuit to model a lossy interconnect introduces error. Recall that time-domain ringing and plateaus occur due to the impedance mismatch between line driver and transmission line, and multiple wave reflections at the output terminal of transmission line. lumped circuits are not able to model the wave reflection phenomenon, which in turn leads to errors in the time and frequency domain estimations of the line. However, this error is negligible under the practical range of values for the line geometries and clock frequency. To verify this, the circuit in Fig. 10 is simulated using HSPICE. To highlight the accuracy of the RLC-π circuit, a wire-length of 4mm is chosen, which is longer than the unbuffered lengths used in practice. The interconnect has a per-unit inductance of 870.53 nH/m, a per-unit length

capacitance of 60.57pF/m, and a per-unit length resistance of 41.83Ω/m. The frequency and time domain responses of the voltage at the output terminal of the lossy line is compared with those of the RLC-π circuit. Figures 12 (a) and (b) show results of these comparisons. In the frequency domain, the output voltage of the RLC-π circuit closely matches that of the lossy line up to 40GHz. In the time-domain, the output voltage of the RLC-π circuit exhibits the same propagation delay and rise and fall times compared to the output response of the line.

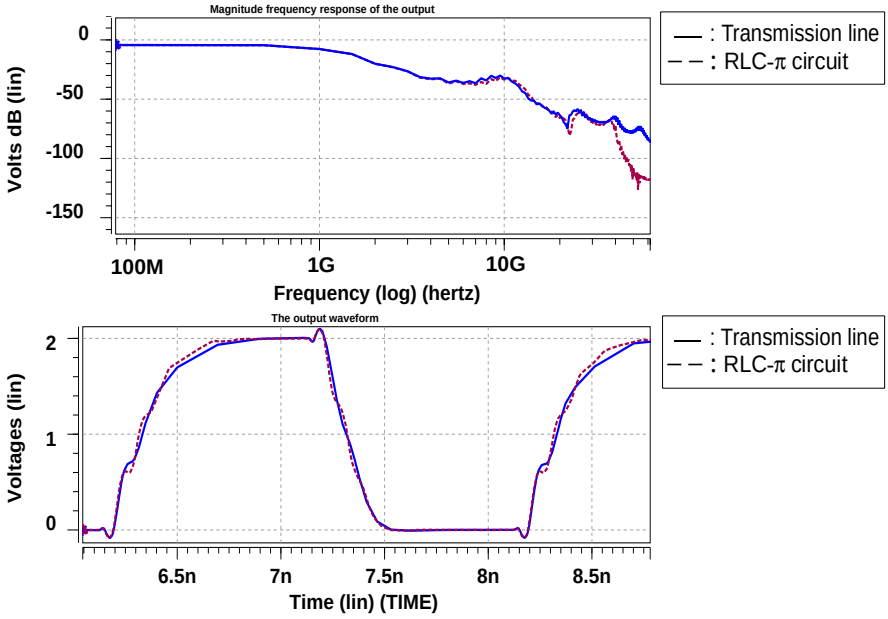


Fig. 12. Frequency and time domain output responses for the circuit of Fig. 10. (a) Frequency domain (b) time-domain waveforms.

The propagation delay of the lossy line is derived using the voltage transfer function $H_v\big|_{x=-h}$. Applying the same second-order truncation as for the impedance on the voltage transfer function, yields:

$$H_v\big|_{x=-h} = \frac{Z_L}{Z_0\cosh(\gamma h) + Z_L\sinh(\gamma h)} \tag{25}$$

The equivalent delay RLC-π model values for $H_v\big|_{x=-h}$ are specified as follows:

$$C_1^D = \frac{C_{int,tot}}{2},\ C_2^D = 0,\ C_3^D = \frac{C_{int,tot}}{2} + C_L\ ,\ L_{eq}^D = L_{int,tot}\ ,\ R_{eq}^D = R_{int,tot}$$

4. DRIVER SIZING FOR OPTIMUM ENERGY-DELAY-RINGING (EDR) PRODUCT

Consider the circuit shown in Fig. 10 consisting of an inverter driving a lossy transmission line. The load is CMOS fanout gates that are connected to the output port of this lossy transmission line and are represented by their input gate-source capacitances. The electromagnetic coupling effects are treated the same way as discussed in Section 3. The output voltage waveform at the load varies significantly as a function of the

driver *W/L* ratio. In practice, the output behavior may change with the driver size and interconnect wire sizing from an overdamped response towards an underdamped response. In other words, although the steady state output voltage values are the same, the transient waveforms are drastically different depending on the electrical parameters of the line and line driver, which is, in turn, a function of the geometrical parameters of the line and line driver. Note that energy dissipation varies as a function of the clock cycle time (equations (3) and (6)). If the output waveform has not reached its steady state at clock edges, the amount of energy dissipation in the clock cycle may be lower (if in the undershoot region) or higher (if in the overshoot region, when exhibiting underdamped behavior) compared to the steady state value of $0.5CV^2$.

V_{out} variations for four different driver *W/L* ratios are shown in Fig. 14. Fig. 15 shows the energy dissipation variation per clock period for different driver *W/L* ratios.

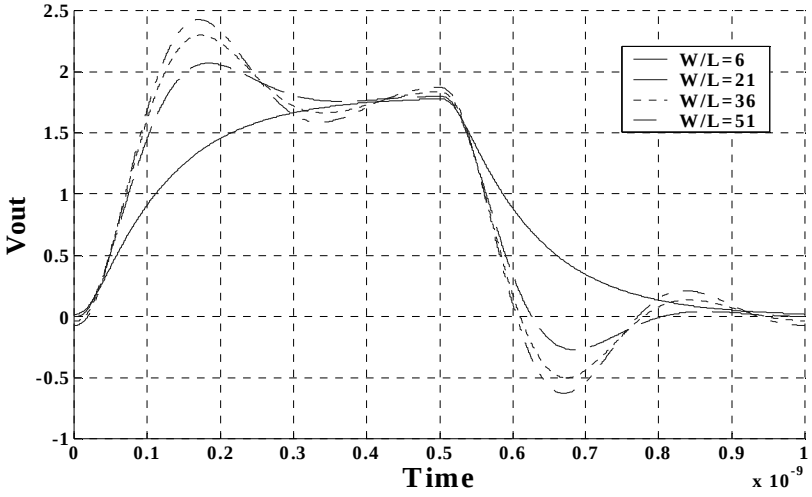


Fig. 13. V_{out} as a function of four different driver *W/L* ratios

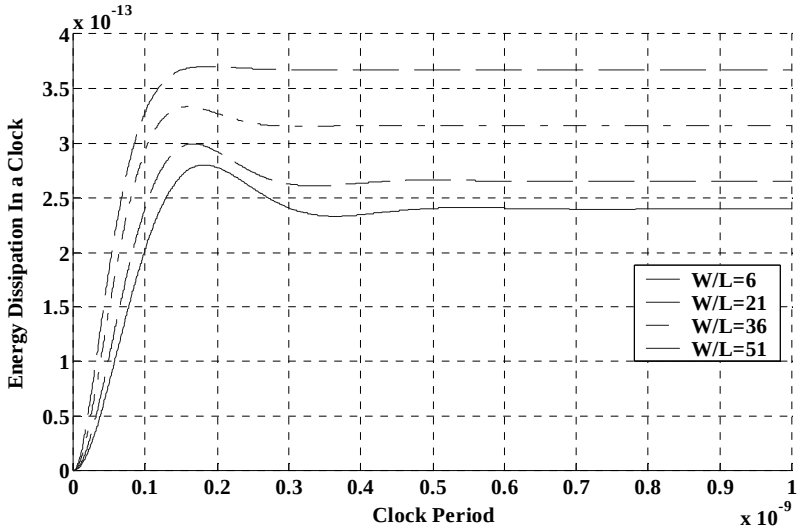


Fig. 14. Energy dissipation in a clock cycle as a function of the clock period for four different driver *W/L* ratios

As a consequence, by changing the *W/L* ratio of the driver we can change the characteristics of the output voltage and thereby, the amount of energy dissipation per clock period. There are three crucial design metrics to consider:

1. Energy dissipation in a clock period
2. 50% propagation delay of V_{out}
3. The signal level of undershoot in an underdamped response which should be less than the noise margin (in a low-to-high transition, the noise margin is approximately the threshold voltage of the PMOS device, $|V_{Tp}|$)

From Fig. 13, one can observe that the overdamped response does not exhibit ringing, but exhibits a larger delay compared to an underdamped response. On the other hand, the underdamped response exhibits lower delay, but may cause DC noise margin violations. Nonetheless, the 50% propagation delay is not a good metric for an underdamped system due to the existence of damped oscillations. To take the effect of the circuit delay into account, we propose a new metric. For the overdamped response since all the waveforms are monotonically rising or falling, the best performance metric is the *energy-50% delay* product. However, for the underdamped response the delay must incorporate the settling time of the oscillations as well as the percentage of maximum undershoot for noise-margin violations. To come up with a unique metric for both the underdamped and overdamped responses, we use the *energy-50% delay*-(*1+undershoot%*) product. Considering "*1+undershoot%*" as ringing factor, we call the cost function, "*EDR* product".

4.1. Analytical Derivation of Output Voltage and Energy Dissipation

[7], [8], and [9] attempted to find the optimum driver size to minimize the *EDR* product. However, they could not find a unified closed-form expression for energy, delay and ringing. Subsequently, they were not able to obtain an analytical solution for the optimum drive size. In contrast, in this paper, we provide a closed-form driver sizing solution that minimizes the *EDR* product.

Consider the circuit in Fig. 10, that is composed of an inverter driving a lossy transmission line. The load is another CMOS gate that is connected to the output port of the lossy transmission line. The electromagnetic coupling effects are treated the same way as discussed in Section 2. Due to the changes in the operation regions of the NMOS and PMOS transistors of the line driver during the low-to-high and high-to-low transitions of the driver's output, we must distinguish between low-to-high and high-to-low transitions of the driver's output. During the low-to-high transition of the driver's output voltage, the PMOS transistor is conducting and provides a low-impedance conduction path from the supply to the load. During the high to low transition of the driver's output voltage, the NMOS transistor is in the "ON" position and no additional energy is transferred out of the power supply.

We calculate the energy transferred out of the power supply during a low-to-high transition. This energy is the total energy dissipated per clock period for a CMOS gate driving another CMOS circuit through a lossy coupled transmission line. The energy delivered by the power supply through the gate in a low-to-high transition of the driver's output voltage is specified as follows:

$$E_{tot} = \int_{(L \to H)} V_{DD}\, i_{DD}(t)\, dt \tag{26}$$

where $i_{DD}(t)$ is the current flowing from the power supply to the load and through the PMOS transistor during the low-to-high transition of the output. The current is obtained using the driving-point admittance of the circuit:

$$I_{in}(s) = \frac{V_{DD}}{s} Y_{in}(s) \tag{27}$$

where $Y_{in}(s)$ is the driving-point admittance seen from the power supply terminal to the source connection of the PMOS transistor of the driver. Fig. 15 shows the equivalent simplified model of the circuit shown in Fig. 10.

As for the inverter, it is known that the operating regions of the conducting transistors change during the input transition. This change of the operating regions makes the analysis cumbersome. As an underlying assumption, the conducting transistors of the driver operate in the triode region for a large portion of the transition time if the line driver has a sufficient current drive capability [10]. As a result, we assume that the conducting transistor will be in the triode region for the entire input transition, and is modeled as an ideal switch in series with its drain-to-source resistance, r_{DS}, along with the equivalent capacitance, C_{diff}. C_{diff} is a parallel combination of the diffusion capacitances of PMOS and NMOS devices (Fig. 15).

The π structure of the RLC-π circuit makes the impedance calculations straightforward. For instance, the diffusion capacitances of the driving CMOS circuits are placed directly in parallel with the capacitor C_1^E of the RLC-π circuitry and consequently, no additional calculation is required.

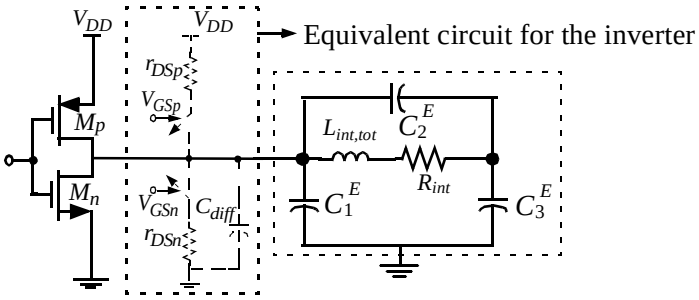


Fig. 15. The equivalent RLC-π circuit model of a lossy coupled transmission line driven by a large CMOS inverter

Considering $C_d^E = C_1^E + C_{diff}$, we, first, derive transfer function of the circuit depicted in Fig. 15:

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{a_2 s^2 + a_1 s + a_0}{b_3 s^3 + b_2 s^2 + b_1 s + b_0} \tag{28}$$

where:

$$a_2 = L_{int,\,tot} C_2^E \qquad a_1 = R_{int} C_2^E \qquad a_0 = 1$$

$$b_3 = r_{DS} L_{int,\,tot} (C_d^E C_2^E + C_d^E C_3^E + C_2^E C_3^E)$$

$$b_2 = L_{int,\,tot} (C_2^E + C_3^E) + r_{DS} R_{int} (C_d^E C_2^E + C_d^E C_3^E + C_2^E C_3^E)$$

$$b_1 = r_{DS} (C_d^E + C_3^E) + R_{int} (C_2^E + C_3^E) \qquad b_0 = 1$$

From Eq. (28) it is readily seen that the system is represented using a third-order transfer function equation. The closed-form analytical solution for energy and delay of a third-order system is too complicated, sometimes the numerical analysis is the only possible solution. On the other hand, as will be explained later, for different interconnect lengths and driver *W/L* ratios, the output voltage of the circuit behaves like a second-order circuit over the frequency range of interest. Several experiments, shown later in this section, using practical geometrical values of an interconnect and line driver in CMOS technology prove that the magnitude of $\left|b_3 \omega^3\right|$ appeared in the transfer function is negligible compared to lower-order coefficients over the frequency range of interest. We can therefore neglect the effect of b_3 and use the 2nd-order approximation as shown below:

$$\frac{V_{out}(s)}{V_{in}(s)} \cong \frac{a_2 s^2 + a_1 s + a_0}{b_2 s^2 + b_1 s + b_0} \tag{29}$$

Using the this approximation, we will find closed-form expressions for the output voltage waveform and the energy of the system.

The above second-order approximation for the third-order denominator of Eq. (28) is valid in nanometer technologies as the device dimensions are scaled down to a few tens of nanometers, because parasitic capacitances of device and interconnect scale down with technology lowering the third-order coefficient b_3 in Eq. (28). r_{DS} increases with the technology scaling, however with smaller scaling factor due to the fact that the mobility degradation and voltage scaling are partially compensated by the reduction of the gate oxide thickness. As an example, Fig. 16 shows the approximated output waveforms for two different wire lengths and driver *W/L* ratios, with an step function at the input of the line driver. The average error between actual output and approximated output waveforms for different interconnect lengths and driver *W/L* ratios is depicted in Fig. 17. The normalized error between the actual output voltage, v_{out}, at the output

terminal of the lossy interconnect driven by CMOS inverter, and the approximated output voltage, $\tilde{v}_{out}$, is calculated as follows:

$$e_N = \frac{\int_0^T [v_{out}(t) - \tilde{v_{out}}(t)]^2 dt}{\int_0^T v_{out}^2(t) dt} \tag{30}$$

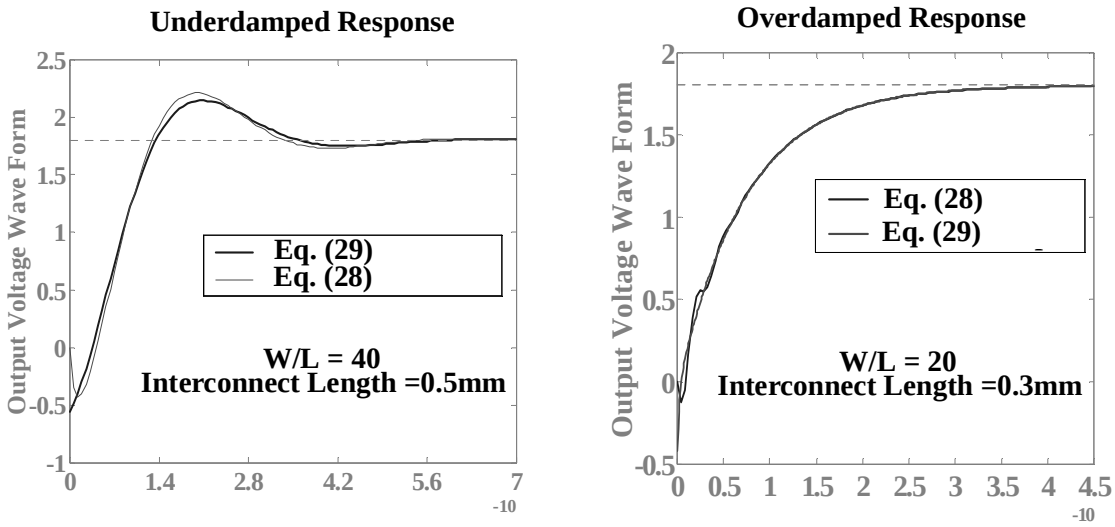


Fig. 16. The comparison between the output voltage calculated using (28) and approximated one using (29) for both underdamped and overdamped cases

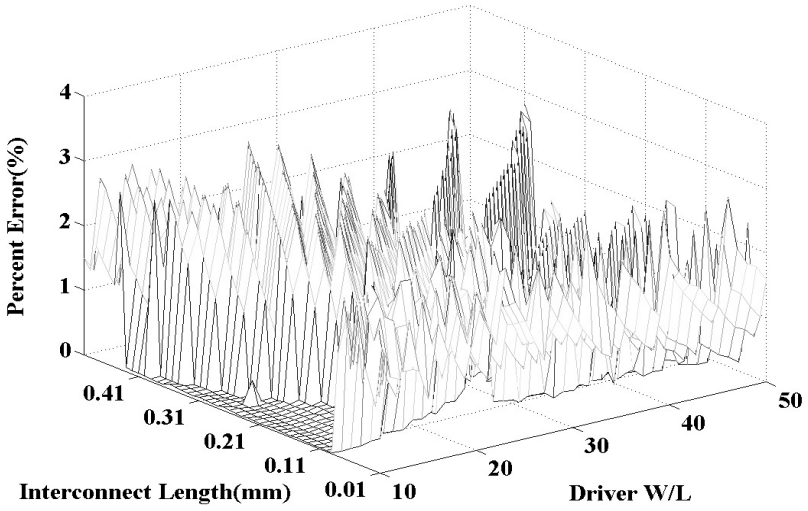


Fig. 17. Average error between real output waveform and approximated waveform

The average error for experimental data derived from 2050 runs of simulations is 0.93% over three different frequency ranges, 1GHz, 1.66GHz, and 2GHz. The maximum error was reported to be 3.4%.

According to the above simulation results, we can use the equivalent second-order approximation and find the output waveform, while introducing a negligible approximation error. Similarly, for the driving point input admittance I_{in}/V_{in} , we have:

$$\frac{I_{in}(s)}{V_{in}(s)} = \frac{d_3 s^3 + d_2 s^2 + d_1 s}{b_3 s^3 + b_2 s^2 + b_1 s + b_0} = \frac{1}{r_{DS}}\left[1 - \frac{L_{int}(C_2^E + C_3^E)s^2 + R_{int}(C_2^E + C_3^E)s + 1}{L_{int}C_2^E s^2 + R_{int}C_2^E s + 1} \times \frac{V_{out}(s)}{V_{in}(s)}\right] \tag{31}$$

where:

$$d_3 = L_{int}(C_d^E C_2^E + C_d^E C_3^E + C_2^E C_3^E)$$
$$d_2 = R_{int}(C_d^E C_2^E + C_d^E C_3^E + C_2^E C_3^E)$$
$$d_1 = C_d^E + C_3^E$$

Substituting the approximated transfer function of (11) in (13), leads to the following:

$$\frac{I_{in}(s)}{V_{in}(s)} = \frac{d_2 s^2 + d_1 s}{b_2 s^2 + b_1 s + b_0} \tag{32}$$

Similar to any second-order circuit, we will distinguish between the overdamped and underdamped responses and analytical models will be derived for both underdamped and overdamped responses.

A. Overdamped Response

In the overdamped case R_{int} and the output resistance of the line driver are sufficiently large so as to eliminate frequency resonance modulated on the current and voltage waveforms. In fact, if $b_1 > 2\sqrt{b_2}$, the equivalent circuit model for the line and line driver in Fig. 16 will exhibit an overdamped response. To obtain the total energy transferred out of the power supply using Eq. (26), the input current to the circuit is first obtained by solving the characteristic differential equation of the RLC-π circuit, which is an over-damped decaying waveform in this case. The voltage response at the output terminal of the RLC-π circuit and the total energy are:

$$v_{out}^{(over)}(t) = V_{DD}[1 + e^{-\alpha_\pi t}(k_1 \sinh(\alpha_{d,\pi} t) + k_2 \cosh(\alpha_{d,\pi} t))] \tag{33}$$

$$E_{tot}^{(over)} = (C_d^E + C_3^E)V_{DD}^2 - V_{DD}^2 \cdot e^{-\alpha_\pi \frac{T}{2}}\left(k_3 \sinh\left(\alpha_{d,\pi}\frac{T}{2}\right) + k_4 \cosh\left(\alpha_{d,\pi}\frac{T}{2}\right)\right) \tag{34}$$

where:

$$k_1 = \frac{a_2}{\alpha_{d,\pi}}\left(\omega_{p,\pi}^2\left(\frac{a_1}{a_2} - \alpha_\pi\right) - \frac{\alpha_\pi}{a_2}\right) \qquad k_2 = a_2\left(\omega_{p,\pi}^2 - \frac{1}{a_2}\right) \qquad k_3 = \frac{d_2}{\alpha_{d,\pi}}\left(\frac{d_1\alpha_\pi}{d_2} - \omega_{p,\pi}^2\right)$$

$$k_4 = -d_1 \qquad \omega_{p,\pi} = \frac{1}{\sqrt{b_2}} \qquad \alpha_\pi = \frac{b_1}{2b_2} \qquad \alpha_{d,\pi} = \sqrt{\alpha_\pi^2 - \omega_{p,\pi}^2}$$

a_i, b_i and d_i are coefficients of the transfer functions V_{out}/V_{in} and I_{in}/V_{in} given in (29) and (32), respectively.

It turns out that if a CMOS inverter driving a lossy coupled line has an overdamped response, and if $\alpha_\pi - \alpha_{d,\pi} >> 4\pi f_{clock}$, then the energy dissipation per each clock period becomes:

$$E_{tot}^{(over)} = (C_d^E + C_3^E) V_{DD}^2 \tag{35}$$

B. Underdamped Response

In the underdamped case, the voltage and current transient waveforms oscillate toward their steady-state values. If $b_1 < 2\sqrt{b_2}$, the current and voltage waveforms will then oscillate until they reach their steady state value. To obtain the total energy transferred out of the power supply Eq. (26) is, once again, employed. The output voltage and the total energy transferred out of the power-supply voltage are as follows:

$$v_{out}^{(under)}(t) = V_{DD}\,[1 + e^{-\alpha_\pi t}(k_1 \sin(\omega_{d,\pi} t) + k_2 \cos(\omega_{d,\pi} t))] \tag{36}$$

$$E_{tot}^{(under)} = (C_d^E + C_3^E) V_{DD}^2 - V_{DD}^2 \cdot e^{-\alpha_\pi \frac{T}{2}} \left(k_3 \sin\left(\omega_{d,\pi} \frac{T}{2}\right) + k_4 \cos\left(\omega_{d,\pi} \frac{T}{2}\right) \right) \tag{37}$$

where the mathematical expressions for k_1, k_2, k_3, k_4, $\omega_{p,\pi}$, α_π are the same as the ones described above and $\omega_{d,\pi} = \sqrt{\omega_{p,\pi}^2 - \alpha_\pi^2}$.

It is seen that if a CMOS inverter driving a lossy coupled line undergoes an underdamped oscillatory response, and if $\alpha_\pi >> 4\pi f_{clock}$, then the energy expression becomes:

$$E_{tot}^{(under)} = (C_d^E + C_3^E) V_{DD}^2 \tag{38}$$

❐

4.2 Analytical Derivation of Delay and Ringing

Earlier in Section 4, a new cost function named *EDR* product was proposed for the purpose of providing a unifying definition of the energy-delay product for both underdamped and overdamped responses of the circuit. To find the optimum point in *EDR* product, we also need to find the 50% delay and ringing. However, calculating these time-domain parameters is straightforward, once we have the voltage response of the circuit in Fig. 15. The 50% propagation delay for any of two possible responses (i.e., underdamped and overdamped) is calculated by setting $V_{out}=V_{DD}/2$ in (15) and (16), respectively.

No ringing phenomenon exists for the overdamped case. For the underdamped case, the ringing is defined as the time at which the output waveform experiences its first minimum value, which is given by:

$$Ringing = 1 + \frac{V_{out}\left(\frac{4\pi}{\omega_d}\right)}{V_{DD}} \tag{39}$$

4.3 Driver Sizing for Optimum *EDR* Product

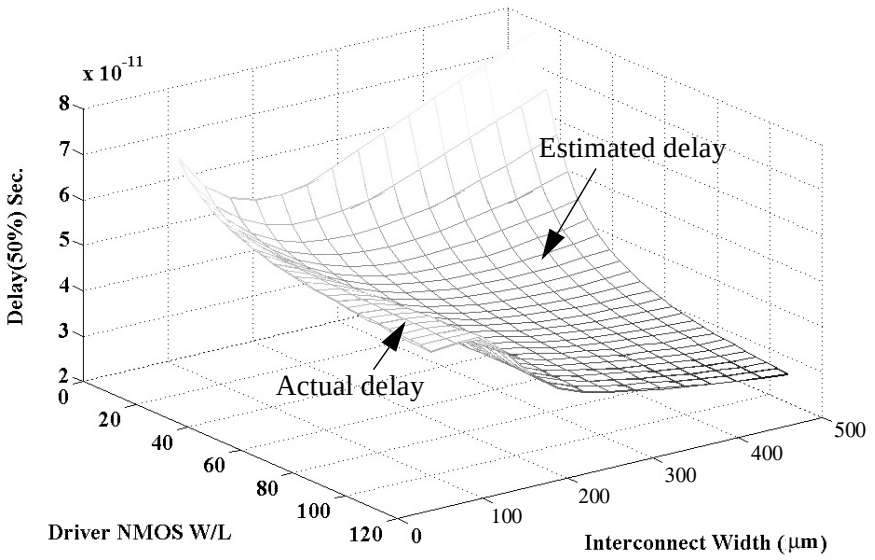
Using equations (34), (37), and (39), the *EDR* product is calculated for the equivalent circuit shown in Fig. 15 that models a lossy interconnect driven by CMOS inverter. Consider $R_D=k_R/W_D$ and $C_{diff}=k_C W_D$, where k_R and k_C are constants that are dependent on the technology, and W_D is the driver size. The optimum driver size is derived by solving the following equation:

$$\frac{d}{d(W_D)}(EDRP) = 0 \tag{40}$$

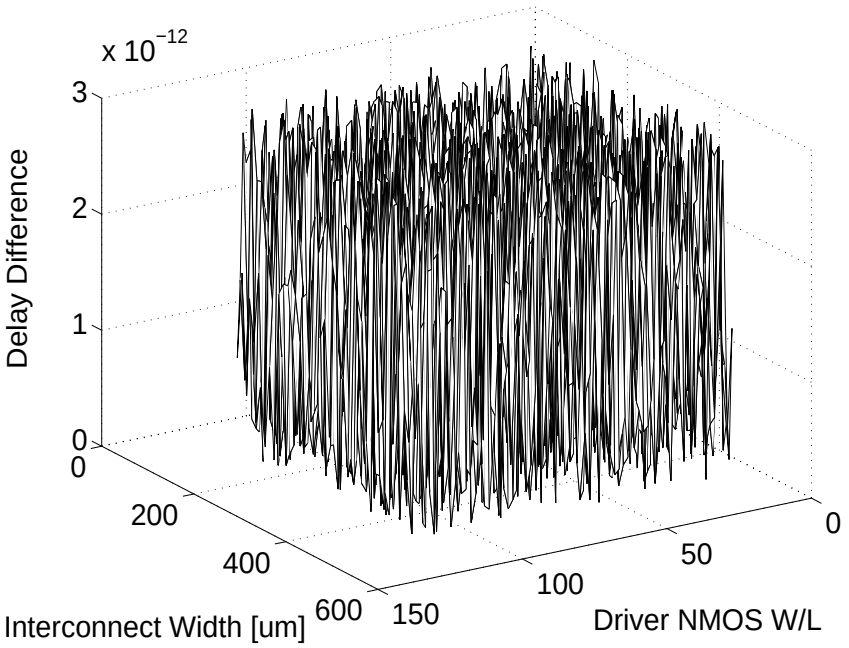
Eq. (40) is a nonlinear equation with respect to the driver size. Hence, the optimum solution is obtained using numerical solution of this nonlinear algebraic equation.

Remember that electrical parameters of a lossy transmission line are a function of the geometrical parameters of that line such as wire width, wire thickness and wire length. Similarly, C_{diff} is a function of the MOS gate aspect-ratios. Subsequently, the energy dissipation of a lossy line driven by a CMOS inverter is a function of line and driver physical parameters. Using BSIM3v3 I-V equations for the MOS transistor and accurate closed form expressions derived in [10], the energy is thus expressed in terms of the geometrical parameters of the interconnect and MOS transistors.

Comparison between our analytical models for delay and energy with HSPICE simulations are demonstrated in Figures 18 (a), (b) and 19 (a) (b), respectively. From these experiments, it can be seen that for different interconnect widths and driver sizes, our delay equation exhibits very high accuracy (i.e., only 1.7% average error) and that the energy equation shows a mere 4.3% average error.

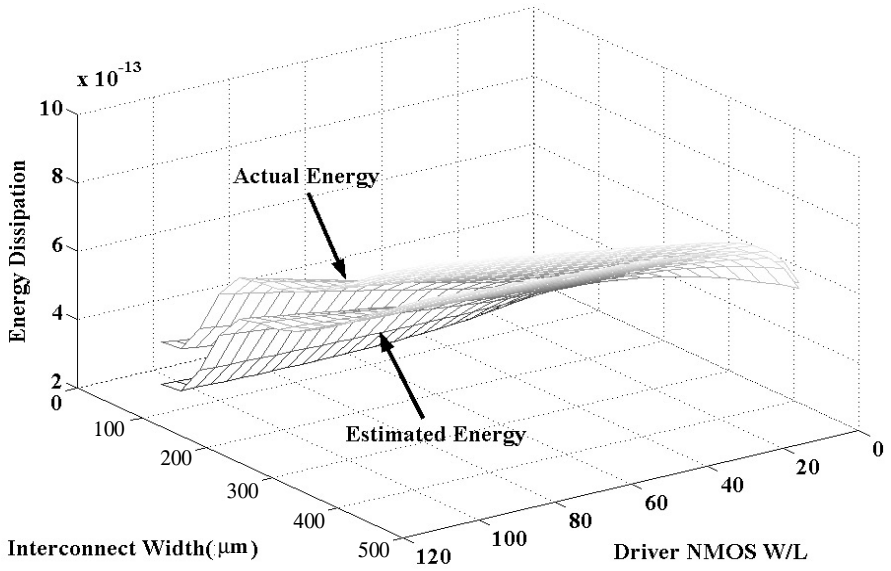


(a)

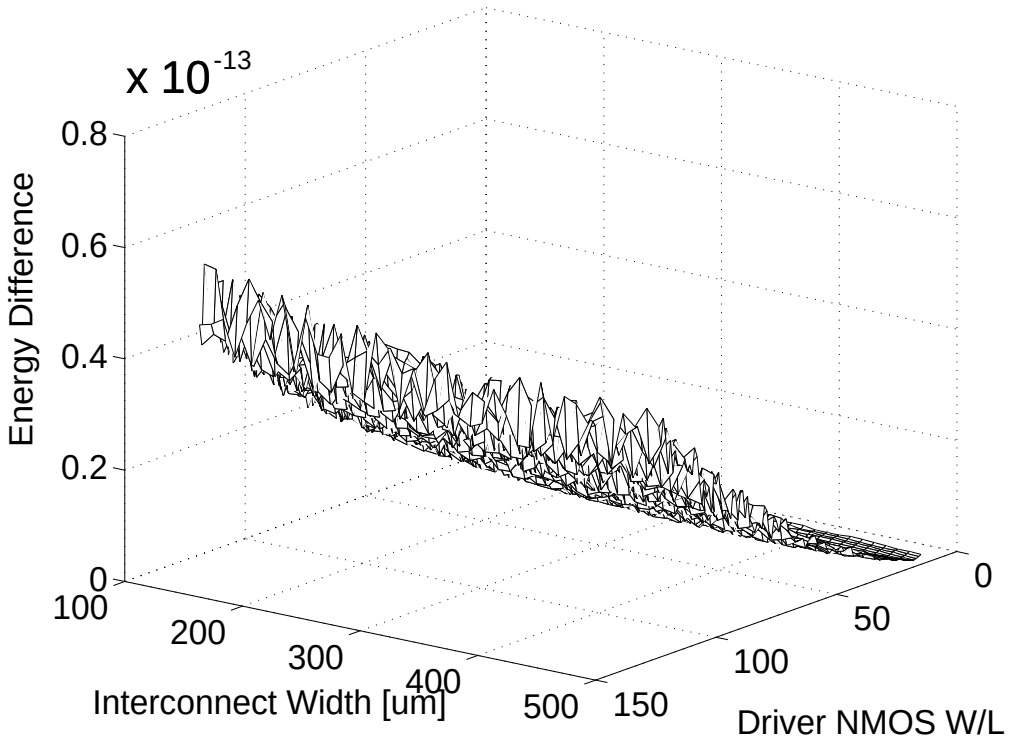


(b)

Fig. 18: (a) Comparison between 50% propagation delay and the obtained formulation for both under-damped and over-damped cases, and (b) difference between the actual delay and the estimated delay



(a)



(b)

Fig. 19. (a) Comparison between actual energy of the lossy line and approximated ones obtained from (34) and (37) for underdamped and overdamped cases, and (b) difference between the actual energy and the estimated energy

Fig. 20 (a) shows the energy variation as a function of the fundamental period, *T*, and for the five different gate aspect-ratios of the driver. The interconnect width is fixed at 5μm. Fig. 20 (b) shows the energy variation with respect to the clock period for the five different values of the metal widths of the interconnect under a fixed driver W/L of 60. The input is a periodic rectangular voltage signal. Note that for small clock periods, the $(1/2)CV^2$ energy model gives rise to a wrong value.

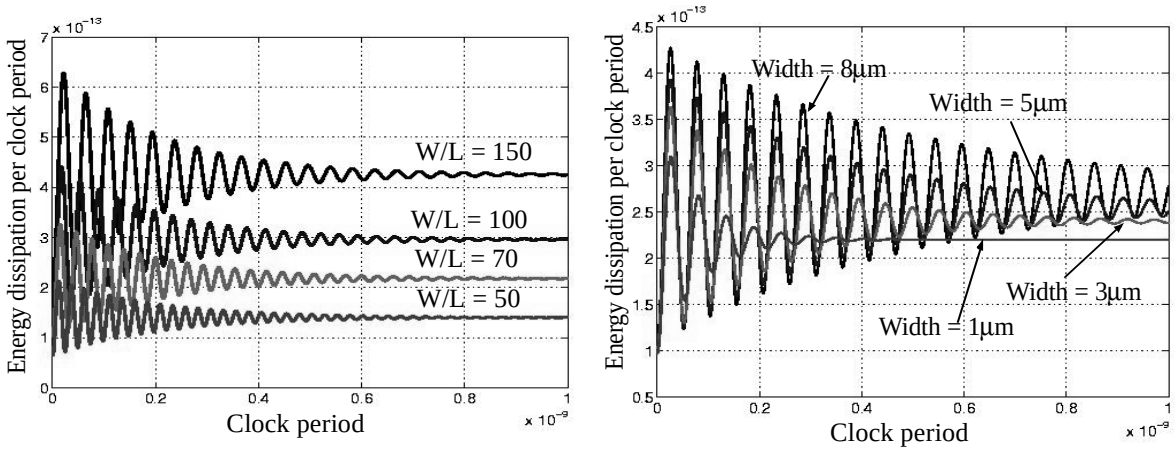


Fig. 20. (a) Energy per clock vs. clock period for six different W/L ratios. (b) Energy per clock vs. clock period for four different interconnect widths (RLC-π).

As the metal width of the interconnect decreases, the transient variations of dissipated energy per clock period in terms of the clock period gradually changes from a damped oscillatory function to a damped exponential function. Note that due to the large gate aspect-ratios, the overdamped response is rarely observed because the line driver's resistance will be very small, in practice. The same statement is true when the W/L of transistors is decreasing. Varying the transistor size and line width will vary the steady-state value of the energy dissipation as being expected. Figures 20 (a) and (b) suggest that for a given clock period, we can change the transistor sizes as well as the interconnect metal width such that the dissipated energy per clock period attains its undershoot value which is beneficial from both the speed and energy point of view. This is, however, a difficult task in practice, because process variations cause a deviation from the optimum undershoot value.

Having accurate expressions for the energy dissipation of a lossy transmission line driven by CMOS drivers helps us propose a new design guideline for an area-efficient wire and transistor sizing to achieve the minimum energy under the noise-margin constraint. However, considering the energy dissipation alone is misleading. In other words, performing wire and transistor sizing to achieve the minimum energy may result in unacceptable delay and insufficient voltage swing, and as a result may lead to the logic and the circuit failures.

Figure 21 shows the *EDR* product per clock cycle of an inverter driving a lossy transmission line with a pure capacitive load termination. The small incremental positive slope of the *EDR* product metric with respect to the *W/L* is due to the direct relationship between the energy and the diffusion capacitance of the device.

As shown in Fig. 21, *EDR* product changes for different driver *W/L* ratios. Furthermore, It is also dependent on the clock period, as domesticated in figures 20 (a) and (b). Fig. 21 shows that for a predetermined interconnect width, there is an optimum driver W/L, which minimizes the *EDR* product.

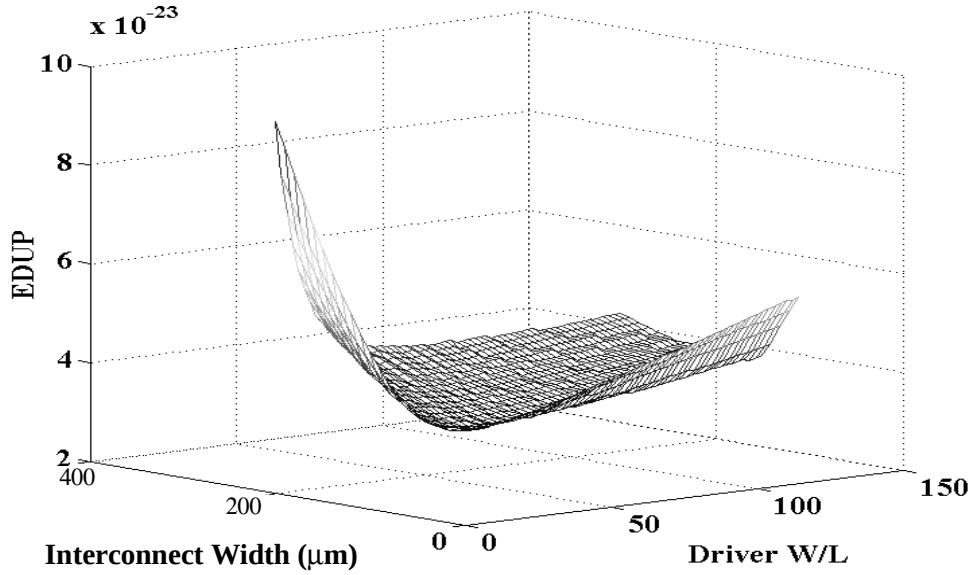


Fig. 21. *EDR* product variation per clock period for different interconnect widths and driver *W/L* ratios

In the energy calculations of interconnects driven by CMOS circuits, it was normally assumed that transients in the current and voltage waveforms have been settled to steady state values and the energy was thus simply equal to $(1/2)CV_m^2$. Section 2.1 and 2.2 showed that this expression can yield quite an inaccurate result for the dissipated energy of the interconnect in high frequency ULSI circuits. Figures 22 and 23 show that modeling a lossy transmission line with a single RLC circuit do not still provide accurate results for energy dissipation analysis of a lone lossy line driven by a large CMOS inverter in both underdamped and overdamped cases. These figures show the dissipated energy of a single lossy transmission line for various line lengths when the line is modeled by the RLC-π circuit and compare it with that obtained using a single RLC circuit. For small clock cycles, the RLC circuit model is unable to give a good energy estimate. This is true for both overdamped and underdamped circuits. Figures 22 and 23 also reveal that for

both underdamped and overdamped circuits when the clock cycle time is sufficiently long, the results obtained by energy calculations in RLC and RLC-π circuits are both closely equal to $(1/2)CV_m^2$.

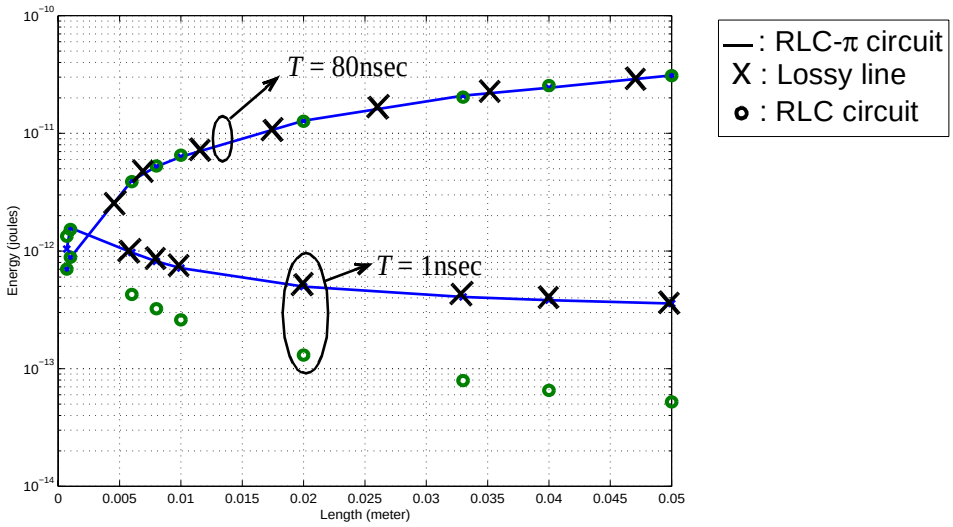


Fig. 22. A comparison between the energy-length variation of the equivalent underdamped RLC-π circuit and that of single underdamped RLC circuit of a lossy transmission line. The comparison has been made for two values of cycle time, T = 1nsec and T = 80nsec

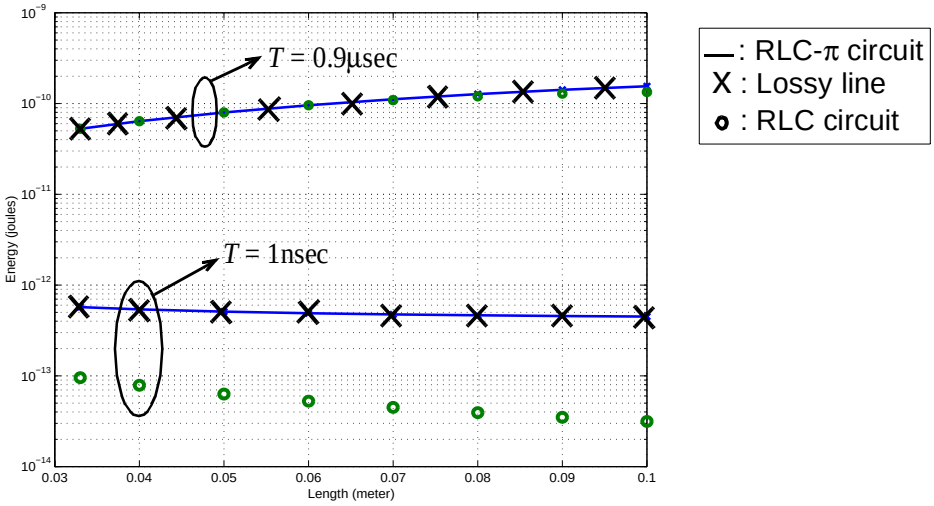


Fig. 23. A comparison between the energy-length variation of the equivalent overdamped RLC-π circuit and that of single overdamped RLC circuit modeling a lossy transmission line. The comparison has been made for two values of cycle time, T = 1nsec and T = 0.9μsec

5. Conclusions

This paper presented accurate expressions for the interconnect energy dissipation and propagation delay in high performance ULSI circuits. We showed that at high clock frequencies, where the output voltage at the termination point of a transmission line, does not reach its steady state value during the clock period, it is possible to reduce energy dissipation while meeting a DC noise margin by driver sizing. It was shown that this phenomenon is mostly due to the voltage behavior of the transmission line at its termination point which may correspond to either underdamped or overdamped behavior. More precisely, if the clock period is chosen such that the output voltage for the underdamped case is in its overshoot region, then energy dissipation per transition in the clock cycle will be higher than $0.5CV^2$. On the other hand, if the output voltage is in the undershoot region when the clock changes, the energy dissipation per transition in the clock cycle will be lower than $0.5CV^2$. Of course for the overdamped case, energy is always less than or equal to $0.5CV^2$. In addition, we propose a new design metric which is the product of energy, delay, and ringing in lossy transmission lines. This metric is used during the driver sizing problem formulation.

6. References

[1] V. De and S. Borker, ”Technology and Design Challenges for Low Power and High Performance”, *ISLPED 99*

[2] J. A. Davis, R. Venkatesan, A. Kaloyeros, M. Beylansky, S. J. Souri, K. Banerjee, K. C. Saraswat, A. Rahman, R. Reif, and J. D. Meindl, "Interconnect Limits on Gigascale Integration (GSI) in the 21st Century," *Proceedings of the IEEE*, *Special Issue on Limits of Semiconductor Technology*, Vol. 89, No. 3, pp. 305- 324, March 2001.

[3] T. Uchino, J. Cong, "An Interconnect Energy Model Considering Coupling Effects," *Proceedings of IEEE/ACM Design Automation Conference*, pp. 555-558, Las Vegas, June 2001.

[4] A. Deutsch, P. W. Coteus, G. Kopcsay, H. Smith, C. W. Surovic, B. Krauter, D. Edelstein, P. Restle, "On-chip Wiring Design Challenges for Gigahertz Operation," *Proceedings of the IEEE*, Vol. 89, No. 4, pp. 529- 555, April 2001.

[5] C. N. Taylor, S. Dey, Y. Zhao, "Modeling and Minimization of Interconnect Energy Dissipation in Nanometer Technologies," *Proceedings of IEEE/ACM Design Automation Conference*, pp. 754-757, Las Vegas, June 2001.

[6] B. Razavi, *Design of Analog CMOS Integrated Circuits*, pp. 166-167, McGraw-Hill, 2001.

[7] P. Heydari, S. Abbaspour, M. Pedram, A comprehensive Study of Energy Dissipation in Lossy Transmission Lines Driven by CMOS Inverters,” *IEEE Custom Integrated Circuits Conf.*, pp. 517-520, May 2002.

[8] Payam Heydari, "Energy Dissipation Modeling of Lossy Transmission Lines Driven by CMOS Inverters," *IEEE International Symposium on Circuits and Systems*, Scottsdale, Arizona, May 2002.

[9] Payam Heydari and Massoud Pedram, "Interconnect Energy Dissipation in High-Speed ULSI Circuits," *IEEE VLSI Design / ASP-DAC Conference*, pp. 132-137, Bangalore, India, January 2002.

[10] S.-M. Kang, Y. Leblebici, *CMOS Digital Integrated Circuits Analysis and Design*, pp. 196-204, McGraw-Hill Companies, Inc., 1999.

Responses to Reviewers' Comments (2nd revision)

Review Number 1
****

Comment:

Page 2, line 3: "one million transistor e will deliver"

Page 2, line 17: "into account for in the energy calculation"

Page 4, line 11: The reference to eq. (5) belongs to the old part of text omitted in this new version, thus making inconsistent the entire statement at the bottom of page 4

Response:

Done. Thank you.

Comment:

Page 5, Fig.2: this figure was overlooked in the previous review. The caption refers to the total delivered energy that should tend to CVm2 for large values of T, not to ½ CVm2; in the figure, also the value of Vm and of the length of the line should be reported, together with r, l, c, to allow a numerical verification of the curve and of the over- or under- dumped condition.

Response:

The caption refers to the total delivered energy, as you correctly mentioned. The steady-state value of the total delivered energy is thus equal to CV_m^2*, as you also pointed out. The wire length for both figure 2 and 3 is chosen to be 2cm. The value for the Vm is 1.8V. All these values have been added in the legends of figures 2 and 3 to add more clarity.*

Comment:

Page 11, line 9: The reference to eq. (20) belongs to the old text; in the new it should be eq. (15)

Page 12, line 20: The reference to eq. (18) should be to eq. (17)

Response:

Done. Thank you

Comment:

Page 13, Fig. 9: There is no mention in text about the comparison of eq. (15) and (21) for impedance approximation of the 0.5mm line; also in the figure eq. (21) for 0.5mm is not visible.

Response:

For the wire-length of 0.5mm, Eq. (21) accurately follows the frequency variation of the actual input impedance given by Eq. (15) over the whole frequency range of Fig. 9. The differences are indistinguishable.

Comment:

Page 17, Fig. 14: The different W/L curves in the figure are not distinguishable in the legend

Page 24, Fig. 18: The interconnect width should be expressed in [um], not in [mm]

Page 25, Fig. 19: Same as for Fig.18

Page 27, Fig. 21: There should be "Interconnect width [um]"

Response:

We modified Figs. 14, 18, 19, 21 to address the above comments. Now the interconnect widths are all expressed in terms of um. Spacing between the legends have been increased in the new revision.

Review Number 2
****

Comment:

page 2, line 3: 'transistor e ': remove the e

page 2, middle: 'into account for': remove the for

page 3, line 1: 'a new RLC', remove new

page 3, line 2: 'sipation, or a': replace or by at

page 4, eqn. 2: i_u is not defined in fig 1

Response:

Thank you. We fixed the typos mentioned above. As for $i_u(t)$*, it is the current flowing through the underdamped circuit [in Fig. 1, i(t) =* $i_u(t)$*].*

Comment:

page 4, 1st line after eqn 2, 'From Eq.(5)' should be Eq. 2

page 5, line 1 after eq 4, 'As T becomes increases' replace by When T tends to infinity

page 5, 1st line of 2.2, 'such that it eliminates' replace by to eliminate

page 6, line before fig 3: 'the underamped response is ....' replace by: 'the underdamped response occurs more frequently in practical situations, because the on chip ....'

page 6, 2 lines before 2.3: 'equations (11) and (12)', should be 'equations (6) and (7)'

page 6, in 2.3, 'a unit step' add of amplitude Vm

page 7, before eqn 9 'of an RLC cicuit' replace by 'of the circuit'

page 11, line 3: 'coupling non-adjacent' to 'coupling of non-adjacent'

page 11, line 4 'have the identical geometries' remove 'the'

page 16 fig 12, horizontal axes for frequencies should read 100M 1G 10G

page 16 line 1 below fig: replace the start of line by The propagation delay ....

page 16 line 2 below fig: after truncation, add 'as for the impedance'

page 17 fig 14, the legend does not allow to determine the figure

Response:

All of the above corrections/comments have been added in the new revision. Thank you.

Comment:

page 18 Vtp is not defined

Response:

VTP is the threshold voltage of the PMOS device as is also defined in the new revision.

Comment:

page 19, line 2 'of a cmos' to 'for a cmos'
page 19, before [10] place 'if the line driver .... capability' at the end of the sentence

Response:

Done. Thank you.

Comment:

page 20 last paragraph: explain why scaling down the technology helps

Response:

Because parasitic capacitances of device and interconnect scale down with technology lowering the third-order coefficient b_3 in Eq. (28). r_{DS} increases with the technology scaling, however with smaller scaling factor due to the fact that the mobility degradation and voltage scaling are partaillly compensated by the reduction of the gate oxide thickness.

Comment:

page 22 after A. 'sufficiently large,' remove the ',' and add 'to eliminate'
page 24 after eq 40, 'numerical analysis' replace by 'numerical solution'

Response:

The above coorections were added in the new revision. Thank you.

Comment:

page 24, fig 18 I think the delay difference would give a better idea of the error
page 25 fig 19 I think the delay difference would give a better idea of the error

Response:

Per your suggestion two graphs shown in Fig. 18 (b) and 19 (b) were added to the new revision demonstrating the delay and energy difference, respectively.